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SUPERGEN Wind Hub

Deliverables:
D2.1.1 High-fidelity, open access Simulink model of wind farm and connection
D2.1.2 Report on dynamics.

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A Generic model of a multi-terminal VSC-HVDC network has been constructed using improved modelling techniques. This is an extension of work from the original Supergen Project EP/H018662/1.

The DC Grid Control 2 Report summarises the results of this work, and this has also been published in publications 1 and 2 below.
The model was then used in a piece of joint work with Alstom Grid (now GE) to evaluate network-wide supervisory controllers (so-called Autonomous Converter Control). This work has been published as a conference paper - publication 3 below.

1. Journal: A. Beddard and M. Barnes, Modelling of MMC-HVDC Systems – An Overview, Energy Procedia, vol. 80, 2015, pp. 201-212, DOI: 10.1016/j.egypro.2015.11.423, (was at 12th Deep Sea Offshore Wind R&D Conference, EERA DeepWind'2015)
2. Journal (write-up of work started on EP/H018862/1) Antony Beddard, Mike Barnes and Robin Preece, “Comparison of Detailed Modeling Techniques for MMC Employed on VSC-HVDC Schemes”, IEEE Trans. Power Delivery, vol. 30, no. 2, April 2015, pp. 579-589, DOI: 10.1109/TPWRD.2014.2325065
3. A. Beddard, A. Adamczyk, M. Barnes and C. Barker, HVDC Grid Control System Based on Autonomous Converter Control, IET PEMD Conference, April 2016, Glasgow https://www.research.manchester.ac.uk/portal/files/31785654/2016_PEMD_Beddard.pdf

DC Grid Control 2 Report

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May 2015

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Acknowledgements

The authors would like to acknowledge the significant contributions that Andrzej Adamczyk, Robert Whitehouse and Carl Barker have made to this work. The authors would also like to thank Wenyuan Wang and Bin Chang for their useful discussions.

Nomenclature

List of Acronyms

AC	Alternating Current
ACC	Autonomous Converter Control
AVM	Average Value Model
AWC	Atlantic Wind Connection
CBC	Capacitor Balancing Controller
DC	Direct Current
DC-XLPE	Direct Current Cross-Linked Polyethylene
DEM	Detailed Equivalent Model
EMS	Energy Management System
EMT	Electromagnetic Transient
EMTDC	Electromagnetic Transients Including DC
FDPM	Frequency Dependent Phase Model
FS	Firing Signal
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LRSP	Load Reference Set-Point
MMC	Modular Multi-level Converter
MT	Multi-terminal
MTDC	Multi-terminal Direct Current
NAWC	Northern section of the Atlantic Wind Connection
NLC	Nearest Level Control
NR	Newton Raphson
ODIS	Offshore Development and Information Statement
PCC	Point of Common Coupling
PFS	Power Flow Solver
SCR	Short-circuit Ratio
SM	Sub-module
VSC	Voltage Source Converter
WP	Work Package
XLPE	Cross-Linked Polyethylene

List of Main Symbols

Symbol	Definition	S.I. Units
BRK	AC Breaker	-
BW_{ic}	Bandwidth of inner current controller	rad/s
BW_{p}	Bandwidth of power controller	rad/s
C	Capacitance	F
C_{eq}	MMC equivalent capacitance	F
C_{SM}	Sub-module capacitance	F
G	Conductance	S
I	Current	A
$I_{(abc)}$	Phase currents	A
I_{arm}	Arm current	A
I_{circ}	Circulating current	A
I_{dc}	DC current	A
I_{dq}	dq current	A
$I_{sx(abc)}$	Phase currents at PCC x where x = 1 to 4	A
K_{droop}	Droop gain for ACC	-
K_{i}	Integral gain	-
K_{p}	Proportional gain	-
L	Inductance	H
L_{arm}	Arm inductance	H
L_{s}	System inductance	H
L_{T}	Transformer inductance	H
N	Number of sub-modules	-
NL	Number of levels	-
N_{p}	Number of turns on the primary winding	-
N_{s}	Number of turns on the secondary winding	-
p	d/dt	-
P	Active power	W
P_{dc}	DC power (+ for power exported to AC system)	W
$P_{dcrated}$	DC rated power	W
P_{w}	Windfarm active power	W
Q	Reactive power	VAr
Q_{w}	Windfarm reactive power	VAr

R	Resistance	Ω
R_{arm}	Arm resistance	Ω
R_{brak}	Braking resistor	Ω
R_T	Transformer resistance	Ω
s	Laplace operator	-
S_{dq}	dq apparent power	VA
τ	time constant	S
T_i	Integral time constant	S
ν	Wind speed	m/s
V	Voltage	V
$V_{c(abc)}$	Internal converter phase voltages	V
$V_{c(dq)}$	dq converter voltage	V
V_{dc}	DC voltage	V
V_{dco}	DC voltage order for DC voltage controller	
V_{dq}	dq voltage	V
$V_{n(abc)}$	Network phase voltages	V
$V_{s(dq)}$	dq voltages at PCC referred to primary converter winding	V
V_{SM}	Sub-module voltage	V
$V_{sx(abc)}$	Phase voltages at PCC x where x = 1 to 4	V
V_{Tp}	Transformer primary winding voltage	V
V_{Ts}	Transformer secondary winding voltage	V
$V_{u(abc)}$	Upper arm phase voltages	V
$V_{w(dq)}$	dq windfarm voltage	V
$V_{x(abc)}$	Output phase voltages for converter x, where x = 1 to 4	V
W	Energy	J
x^*	Set-point	-
$\tilde{x}$	Error	-
$\hat{x}$	Peak	-
X	Reactance	Ω
X_T	Transformer leakage reactance	Ω
Y	Admittance	S
Z	Impedance	Ω
Z_n	Network impedance	Ω
ω	System frequency	rad/s
ω_n	Natural frequency	rad/s

Executive Summary

The aim of this report is to outline the work that has been carried out for the "DC Grid Control 2" Work Package. The objective of this WP is to further develop and verify the DC grid control concepts which were initially proposed by Alstom Grid in 2010. This involves giving a clear description of the different DC grid control layers and implementing these control layers to assess their performance to various events.

In this report, the main layers of the overall DC grid control architecture have been described. The key interface signals between the different control layers and their bandwidths have been defined for this work. A power flow solver has been developed in MATLAB with a PSCAD interface. The solver is shown to be able to accurately calculate the target DC converter voltages required to obtain the desired power flow, without exceeding the nominal operating limits of the system. A method for selecting the droop gain for the Autonomous Converter Controllers (ACC) to prevent operating frame violations is also proposed.

A six terminal HVDC grid model, based on the DC configuration for the Northern section of the Atlantic Wind Connection (NAWC) has been developed in PSCAD. The grid consists of six 1GW VSC converters which are represented using average value models. The three onshore VSCs are connected to simplified traditional AC systems and the three offshore VSCs are connected to 1GW windfarms. The control systems required for the VSCs connected to traditional AC networks have been implemented based on ACC, which was originally proposed by Alstom Grid.

The developed model has been simulated for a range of tests including wind power variations and converter blocking. The simulation results show that the HVDC control system is able to accurately control DC power flow in steady-state and to maintain grid stability for transient events without violating the system's operating frame.

1 Introduction

The purpose of this report is to outline the work that has been carried out for the "DC Grid Control 2" Work Package (WP). The objective of this WP is to further develop and verify the DC grid control concepts which were initially proposed by Alstom Grid in 2010 [1, 2].

The overall DC grid control architecture which has been proposed by Alstom Grid has yet to be formally described or implemented. A key objective of this WP is therefore to formalise the grid controller architecture. This includes a clear description of the different DC grid control layers including their interface signals and bandwidths.

The DC grid control work which has been conducted so far has focused on the main control principles operating under normal conditions. This work therefore looks at the supplementary control layers, such as the DC power flow solver and converter control, when the DC grid is working near the limit of its operating frame.

2 Grid Control Architecture Overview

An overview of the simplified grid control architecture is shown in Figure 1. A HVDC grid could be connected to one or more AC systems. These AC systems could be a mixture of traditional onshore AC networks, windfarm power plants and passive loads. It should be noted that this figure only shows an example of a DC grid control architecture and that it does not include every potential signal between the different control layers.

The Energy Management System's (EMS) key function is to determine the DC power (P_{dc}*) orders for each VSC. In order to do this, the EMS requires DC grid data and information from the connected AC systems. The EMS could issue DC power orders to the Power Flow Solver (PFS) based on energy transfer agreements between the connected AC systems. The EMS could also provide services such as AC frequency regulation at an additional cost. If the requested power orders are likely to result in the HVDC grid operating near to its limits, an error message is sent to the EMS resulting in a new set of power orders.

The droop gain (K_{droop}) for each converter affects how much the power of that converter changes due to a transient event. Some AC system operators may wish to pay to have a droop gain which results in minimal power variation, while other system operators could be compensated for taking a bigger proportion of the power change. The droop gain settings would be set by the EMS.

The main function of the PFS is to calculate the target DC voltage (V_{dc}*) for each node, in order to obtain the target DC node powers without exceeding the operating limits of the equipment within the DC grid. The PFS sends the DC voltage order, DC power order and droop gain setting to each VSC's control system. The VSC control systems manipulate their AC converter voltage references (V_{ac}*) to achieve the target DC voltage and local reactive power order (Q*).

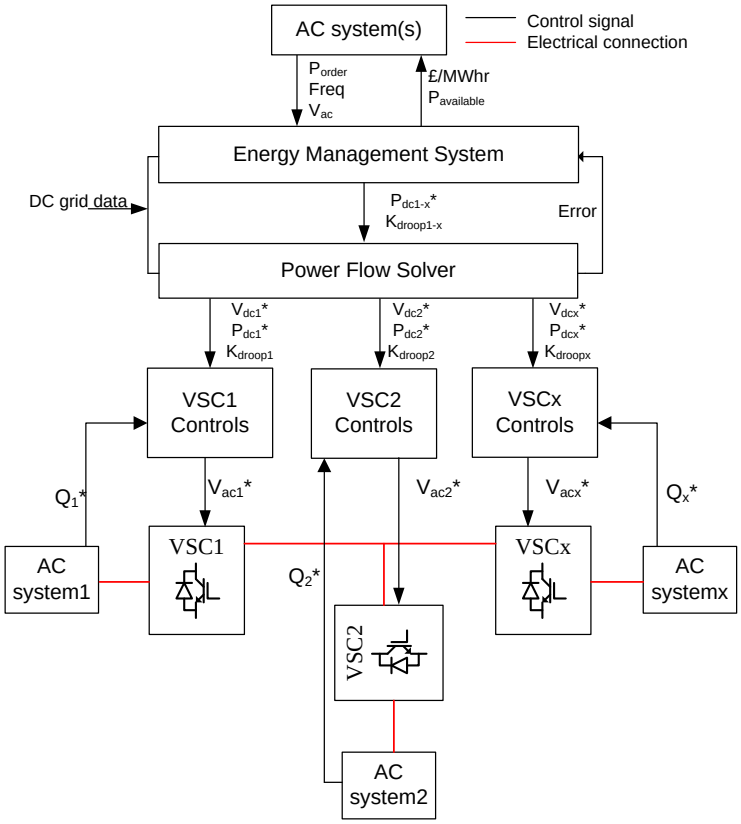

Figure 1: Example DC Grid Control Architecture

The focus of this work is on control architecture below the EMS, since the development of the EMS is highly dependent upon policy and is therefore considered to be out of the scope of this Work Package (WP). To aid understanding, the design of the control architecture will be described in relation to the Northern section of the Atlantic Wind Connection (NAWC).

3 Northern Atlantic Wind Connection Model

A model based on the DC configuration for the NAWC has been implemented in PSCAD and is shown in Figure 2. The grid consists of three 1GW offshore windfarms which are connected to three 1GW offshore VSCs. The offshore VSCs are connected together via two pairs of HVDC cables (20km and 30km) and to the three onshore 1GW VSCs via three pairs of HVDC cables (200km, 50km and 50km). The DC voltage for the NAWC is

expected to be around 600kV. The onshore MMCs are connected to three strong simplified AC systems. The onshore AC systems are not based on the New York/New Jersey power system. The key parameters for this model are given in the Appendix A.

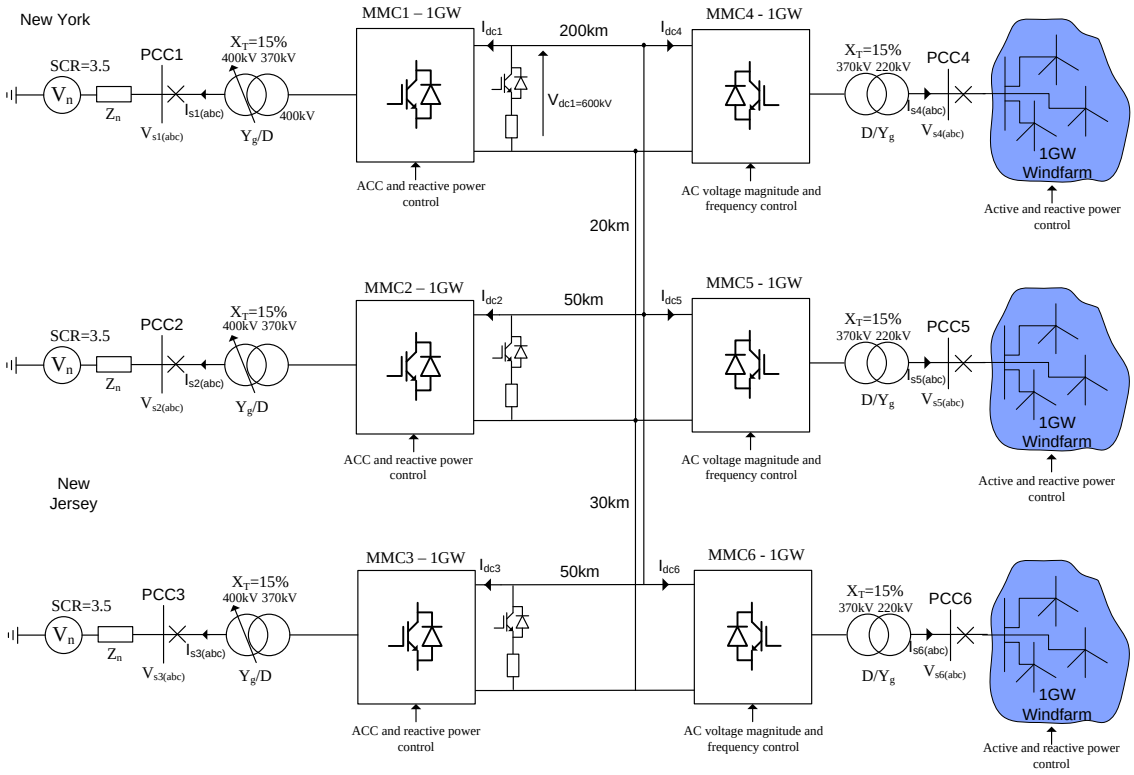

Figure 2: Test model based on the DC configuration for the northern section of the AWC

3.1 Voltage Source Converter

Since its inception in 1997 and until 2010 all VSC-HVDC schemes employed two or three level VSCs [3]. In 2010, the Trans Bay cable project became the first VSC-HVDC scheme to use Modular Multi-level Converter (MMC) technology. The MMC has numerous benefits in comparison to two or three level VSCs; chief among these is reduced converter losses. Today, the main HVDC manufacturers offer a VSC-HVDC solution which is based on multi-level converter technology.

It is assumed that the AWC would employ the Half-Bridge (HB) MMC since the advantages of fault blocking converters for DC cable systems is not yet apparent. The basic structure of a three-phase HB-MMC is shown in Figure 3. Each leg of the converter consists of two converter arms which contain a number of Sub-Modules (SMs), and a reactor, L_{arm}, connected in series. Each SM contains a two-level HB converter with two IGBTs and a parallel capacitor. The module is also equipped with a bypass switch to remove the module from the circuit in the event that an IGBT fails, and a thyristor, to protect the lower diode from overcurrent in the case of a DC side fault.

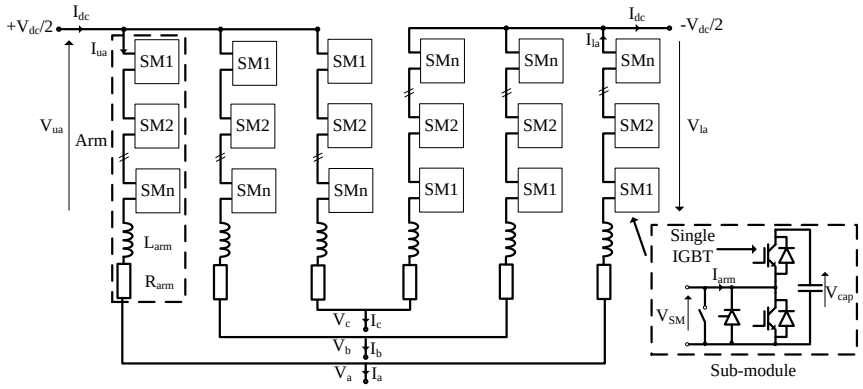

Figure 3: Three-phase HB-MMC

The SM terminal voltage, V_{SM}, is effectively equal to the SM capacitor voltage, V_{cap}, when the upper IGBT is switched-on and the lower IGBT is switched-off. The capacitor will charge or discharge depending upon the arm current direction. With the upper IGBT switched-off and the lower IGBT switched-on, the SM capacitor is bypassed and hence V_{SM} is effectively at zero volts. Each arm in the converter therefore acts like a controllable voltage source, with the smallest voltage change being equal to the SM capacitor voltage. The converter output voltages, $V_{(a,b,c)}$, are effectively controlled by varying their respective upper and lower arm voltages, $V_{u(a,b,c)}$ and $V_{l(a,b,c)}$ as described by equation (1) for phase A [4].

$$V_a = \frac{V_{la} - V_{ua}}{2} - \frac{L_{arm}}{2}\frac{dI_a}{dt} - \frac{R_{arm}}{2} I_a \qquad (1)$$

The number of discrete voltage levels the MMC is able to produce is dependent upon the number of SMs in the converter arms. As the number of SMs increase, the harmonic content of the output waveform decreases. Commercial MMC-HVDC schemes contain hundreds of SMs per converter arm [5]. The primary reason that such a large number of SMs per converter arm are required is to reduce the voltage stress across each SM to a few kV, it is however possible to use significantly less SMs and still not require AC filters. The HB-MMCs employed for the model have a nominal power rating of 1GW at 600kV (±300kV).

The choice of the SM capacitance value, C_{SM}, is a trade-off between the SM capacitor ripple voltage and the size of the capacitor. A capacitance value which gives a SM voltage ripple in the range of ±5% is considered to be a good compromise [6]. The analytical approach proposed by Marquardt et al. in [7] was used to calculate the approximate SM capacitance required to give a ±5% voltage ripple for a 1GW converter.

The converter arm currents consist of three main components as given by equation (2) for phase A. The circulating current, I_{circ}, is due to the unequal DC voltages generated by the three converter legs. The circulating current is a negative sequence (a-c-b) current at double the fundamental frequency, which distorts the arm currents and increases converter losses [8].

$$I_{ua} = \frac{I_{dc}}{3} + \frac{I_a}{2} + I_{circ} \qquad I_{la} = \frac{I_{dc}}{3} - \frac{I_a}{2} + I_{circ} \tag{2}$$

The valve reactors, also known as converter reactors and arm reactors, which are labelled L_{arm} in Figure 3, have two key functions. The first function is to suppress the circulating currents between the legs of the converter and the second function is to reduce the effects of faults both internal and external to the converter. By appropriately dimensioning the limb reactors, the circulating currents can be reduced to low levels and the fault current rate of rise through the converter can be limited to an acceptable value. As the size of the limb reactor increases, the circuiting current, and the rate of rise of arm current in the event of a DC side fault decreases.

According to [9], the Siemens HVDC Plus MMC converter reactors limit the fault current to tens of amps per microsecond even for the most critical fault conditions, such as a short-circuit between the DC terminals of the converter. This allows the IGBTs in the MMC to be turned-off at non critical current levels. A minimum value of limb reactance to ensure that the arm current does not exceed 20A/μs for the worst case scenario is therefore a good starting point. The limb reactance can then be increased further as a compromise between the size of the reactor and the magnitude of circulating current. The circulating current can also be suppressed by converter control action or through filter circuits [6]. For this work a 45mH (0.1p.u.) limb reactor used in conjunction with a Circulating Current Suppressing Controller (CCSC) was found to offer a good level of performance.

3.1.1 MMC-AVM

There are many different techniques for modelling a MMC [10-12]. These range from very detailed semi-conductor physics based models, which are too complex to model a full MMC, to very simple power flow models. The accuracy and simulation speed of a wide range of MMC models have been compared in numerous publications [10, 11, 13, 14]. Average Value Models (AVMs) are used to represent the HB-MMCs for this work since their accuracy is sufficient for the studies being conducted and they are significantly more computationally efficient than the more detailed models [10]. The MMC-AVM is shown in

Figure 4, where the IGBT switch, S, is closed during normal operation and is open when the converter is blocked.

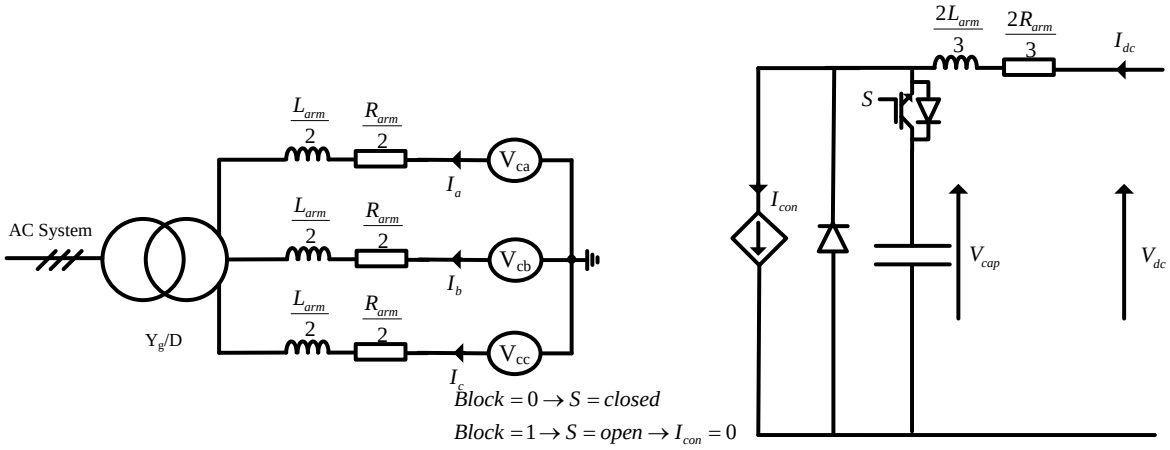

Figure 4: MMC-AVM

The internal converter voltage for phase A, V_{ca}, is given by equation (3) where V_{refca} is the voltage reference generated by the control system, and V_{pg} and V_{ng} are the positive and negative pole to ground voltages.

$$V_{ca} = V_{refca} + \left(V_{pg} + V_{ng}\right)0.5 \tag{3}$$

To account for DC offset $0.5\left(V_{pg} + V_{ng}\right)$ is added to the AC converter voltage references. The internal converter voltages are also limited by the instantaneous values of the positive and negative pole to ground voltages to prevent the AC side of the converter model from generating voltages in excess of the capability of a HB-MMC.

The value for the DC current source, I_{con}, is calculated using equation (4). It should be noted that I_{con} is set to zero when the converter is blocked.

$$I_{con} = \frac{P_{AC}}{V_{cap}} \tag{4}$$

The equivalent capacitance for the AVM, C_{eq}, is 230μF, which is based on the total stored energy of a 600kV, 1GW MMC with a maximum SM capacitor voltage ripple of ±5% . However, it should be noted that only half of the MMCs SM capacitors are in-circuit at any one time during normal operation and hence the MMCs equivalent capacitor during normal operation is 115 μF. The impact of using a single capacitance value to represent the MMCs capacitance is discussed further in section 4.2.3.

The power losses for the AVM can be calculated using equation (5). An arm resistance value of 0.9Ω is employed in the model which represents converter losses of 0.5% at rated power.

$$P_{loss} = 3 \times I_{cjrms}{}^{2} \frac{R_{arm}}{2} + I_{dc}{}^{2} \frac{2R_{arm}}{3} \quad (5)$$

Additional components can be added to the AVM to improve its accuracy for converter energisation and DC fault studies, however neither of these studies are conducted in this work and therefore no further discussion is warranted.

3.2 Onshore AC Network

The strength of an AC system is often characterised by its Short-circuit Ratio (SCR), which is defined by equation (6), where V_n is the network voltage, Z_n is the network impedance and P_{drated} is the power rating of the HVDC system.

$$SCR = \frac{V_n{}^{2}/Z_n}{P_{drated}} \quad (6)$$

An AC system with a SCR greater than three is defined as strong [15]. The SCR of the AC system in this model is selected to be strong with a SCR of 3.5. The AC network impedance is highly inductive and consequently the AC system impedance is modelled using an X/R value of 20. The SCR is implemented in PSCAD using an ideal voltage source connected in series with a resistor and an inductor. The values of resistance and inductance are 2.28Ω and 0.145H (0.34p.u.) respectively.

The winding configuration of the converter transformer in the model is delta/star, with the delta winding on the converter side of the transformer as is the case for the Trans Bay Cable project [16]. A tap-changer is employed on the star winding of the transformer to assist with voltage regulation. The transformer leakage reactance is set to 0.15p.u. with copper losses of 0.005p.u., which are typical values for a power transformer [17]. Power losses per converter station (MMC and transformer) are 1% at rated power for this model. The nominal transformer parameters are given in Table 1, and a simplified diagram of the onshore system is shown in Figure 5.

Transformer parameters				
S (MVA)	V_{Tp} (kV)	V_{Ts} (kV)	L_T (H)	R_T (Ω)
1000	370	410	0.065	0.68

Table 1: Nominal transformer parameters

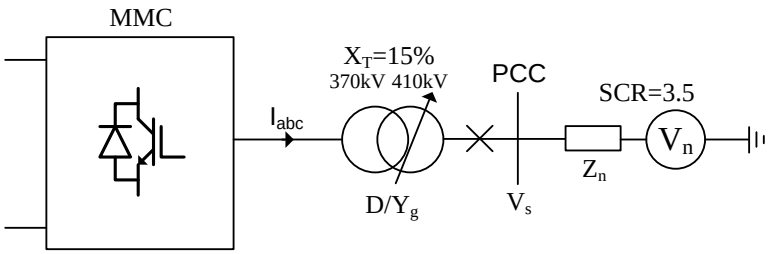

Figure 5: Onshore AC system

3.2.1 HVDC Cable

The system's HVDC cables are rated for a nominal power of 1GW at 300kV. The cables are modelled using the Frequency Dependent Phase Model (FDPM) which is said to be the most accurate and robust cable model commercially available [18]. In the absence of publicly available data for a commercial HVDC cable model, the geometric and material properties for the layers of the cable, which can be represented in the cable model, have been estimated and are given in Table 2.

Layer	Material	Radial Thickness (mm)	Resistivity (Ω/m)	Relative Permittivity	Relative Permeability
Conductor	Stranded Copper	24.9	$2.2\text{x}10^{-8*}$	1	1
Conductor	Semi-conductive	1	-	-	-
Insulation	XLPE	18	-	2.5	1
Insulator screen	Semi-conductive	1	-	-	-
Sheath	Lead	3	$2.2\text{x}10^{-7}$	1	1
Inner Jacket	Polyethylene	5	-	2.3	1
Armour	Steel	5	$1.8\text{x}10^{-7}$	1	10
Outer cover	Polypropylene	4	-	1.5	1
Sea-return	Sea water/air	-	1	-	-

*Copper resistivity is typically given as $1.68*10^{-8}\Omega$/m. It has been increased for the cable model in PSCAD due to the stranded nature of the cable which cannot be taken into account directly in PSCAD.

Table 2: Physical data for a 300kV 1GW submarine HVDC cable

The conductor parameters are based on a stranded copper conductor installed in a moderate climate with close spaced laying [20]. The PSCAD default value for the semi-conducting screen's thickness is employed in this work which is 1mm. There is no official documentation regarding the insulation thickness of the HVDC cables, however a representative from a leading cable manufacturer has stated that a 320kV HVDC cable has an insulation thickness of about 18mm. The representative also stated that using the electrical parameters from an AC cable of similar thickness would yield similar results. This indicates that the relative permittivity of XLPE and DC-XLPE is similar. The relative permittivity of XLPE is given as 2.5 [21]. The relative permittivity of polypropylene yarn is assumed to be very similar to that of polypropylene which is 1.5 [22].

The calculation of the sea-return impedance is complex. In order to calculate the sea-return impedance accurately, accurate values of sea resistivity, sea-bed resistivity, sea depth, cable burial depth and frequency are required. A number of these parameters also vary with the tide and the cable route. PSCAD can only consider the air/sea interface for a submarine cable and therefore only the sea resistivity and cable depth below the sea surface are required. The resistivity of sea water varies in the range of 0.25-2Ωm^{-1} due to the temperature and the salinity of the water [23], which makes it difficult to obtain an accurate value. The sea resistivity and cable depth are assumed to be of 1Ωm^{-1} and 50 metres respectively.

The positive and negative cables may be installed in separate trenches tens of meters apart, to prevent a ships anchor from damaging both cables [24, 25]. This is however approximately 40% more expensive than installing both cables in a single trench, [25] and laying both cables close together means that their magnetic fields effectively cancel out. Unless the cable route has a lot of fishing activity it is therefore more likely that the cables will be buried in a common trench. It has been assumed that the horizontal distance between the two cables would be approximately two cable diameters (0.25m).

The sheath and armour in the submarine cable are bonded to ground at both ends of the cable [24] through a small resistor. The last metallic layer (armour in a submarine cable), is eliminated from the impedance matrix. This is often a valid assumption for a submarine cable, where the armour is a semi-wet construction which allows water to penetrate [26]. The starting frequency for the frequency dependent models is set to 0.1Hz and equal weighting is given to the entire frequency range. The DC correction function is enabled with shunt a conductance value of $1x10^{-10}$ S/m. It should be noted that a 300kV DC-XLPE cable will typically have a shunt conductance value of less than $1x10^{-12}$S/m [27, 28], however using such a small value of shunt conductance increases the likelihood of passivity violations. All other settings are left at their default value.

3.2.2 DC Braking Resistor

DC braking resistors are normally required on VSC-HVDC schemes used for the connection of windfarms [29]. There are situations, such as an onshore AC grid fault, which diminish the onshore converter's ability to export the energy from the windfarm. The bulk of this excess energy is stored in the scheme's SM capacitors leading to a rise in the DC link voltage. The DC braking resistor's function is to dissipate this excessive energy and to therefore prevent unacceptable DC link voltages.

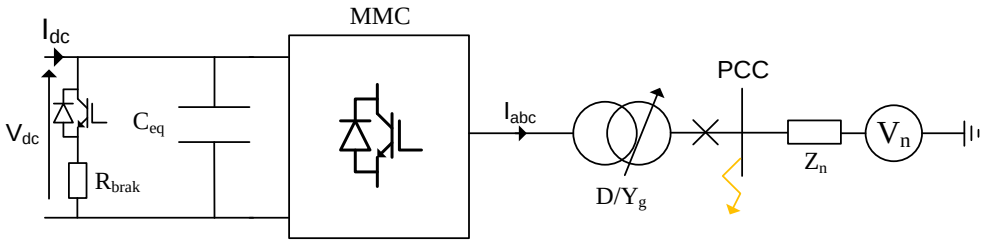

Figure 6: DC braking resistor

The worst case scenario is where the onshore MMC is unable to effectively export any active power. This can occur for severe AC faults such as a solid three-phase to ground fault at the PCC as shown in Figure 6. The braking resistor should therefore be rated to dissipate power equal to the windfarm power rating, P_{wrated}. The braking resistor, R_{brak}, is turned-on once the DC voltage exceeds a set limit (640kV) and is then turned-off once the DC voltage has returned below the set limit (611kV) [29]. These voltage thresholds prevent the braking resistor from interfering under normal operating conditions. In this work, the DC braking resistor is designed to prevent the DC link voltage from exceeding 1.1p.u. and is calculated using equation (7).

$$R_{brak} = \frac{(1.1V_{dcnom})^2}{P_{wrated}} = \frac{660kV^2}{1000MW} = 435.6\Omega \qquad (7)$$

A small safety margin is added by employing a braking resistor of 420Ω for this work. The IGBT braking valve would therefore be required to conduct up to approximately 1.6kA.

3.3 Offshore AC Network

A 1GW offshore windfarm would typically contain 200 wind turbines based on a 5MW turbine design. A simplified diagram of a full scale converter wind turbine is shown in Figure 7. The DC link voltage varies due to the generated power. The function of the grid side converter is to maintain the DC link voltage and to supply/absorb reactive power if required. The power generated by the wind turbines is transmitted at 33kV to two 500MW AC substations which step-up the voltage to 220kV for transmission to the HVDC link.

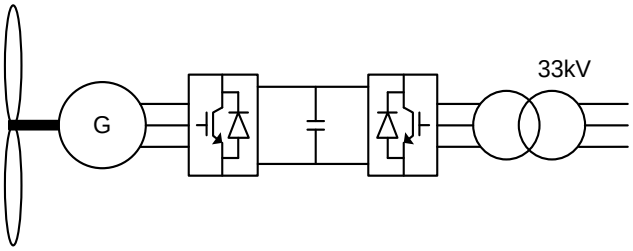

Figure 7: Simplified diagram of a full scale converter wind turbine

The focus of this work is the HVDC scheme, and therefore a simplified representation of the offshore AC system is employed as shown in Figure 8. The voltage sources, V_w, which represent the windfarm generators, are controlled using a dq controller to inject active power into the offshore HVDC converter.

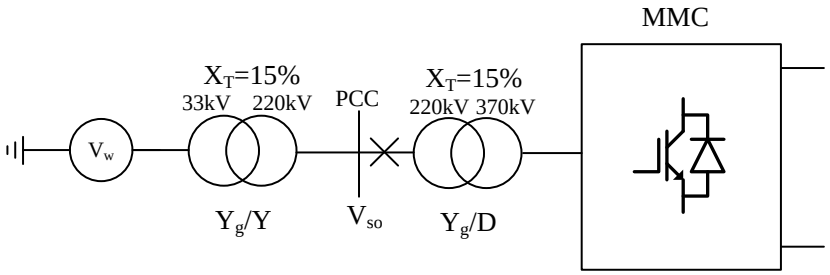

Figure 8: Representation of the offshore network

4 Control Systems

This section describes the numerous control functions which are required for the MMC-HVDC grid.

4.1 Power Flow Solver

In order to calculate the DC node voltages for the given target DC node powers, one DC node voltage must be known. This node is typically referred to as the DC slack bus. The objective of the power flow solver is to determine the node power for the slack bus and the node voltages for the other nodes.

The power injected into node i from the other nodes can be calculated using equation (8). V_i and V_j are the voltages at nodes i and j respectively, Y_{ii} is the self-admittance of node i and Y_{ij} is the branch admittance between nodes i and j.

$$P_i = V_i I_i = V_i \left(\sum_{j=1}^{n} Y_{ij} V_j \right) \tag{8}$$

Using the system shown in Figure 9 as an example, the power at node 1 can therefore be calculated using equation (9).

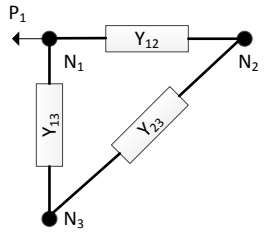

Figure 9: Example system

$$P_1 = V_1 I_1 = V_1 \left(Y_{11} V_1 + Y_{12} V_2 + Y_{13} V_3 \right) \tag{9}$$

Where the admittance of node 1:

$$Y_{11} = -(Y_{12} + Y_{13}) \tag{10}$$

In generalized form, the node powers for a system with n nodes can be calculated using equation (11), where "$.\times$" denotes element-wise multiplication.

$$[P_i] = [V_i] .\times \left([Y_{ij}][V_j] \right) \tag{11}$$

Where:

$$[P_i] = \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_n \end{bmatrix} \quad [V_i] = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} \quad [V_j] = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix} \quad \left[Y_{ij} \right] = \begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1n} \\ Y_{21} & Y_{22} & \cdots & Y_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ Y_{n1} & Y_{n2} & \cdots & Y_{nn} \end{bmatrix} \tag{12}$$

$$Y_{ii} = -\sum_{j=1, j \neq i}^{n} Y_{ij} \tag{13}$$

Equation (11) can be solved using the widely used Newton Raphson (NR) method [30, 31]. The NR method is an iterative solution which requires an initial estimate of the node voltages in order to calculate the injected power at each node. The calculated injected powers at each node are then compared with the target node powers in order to calculate the error. If the error is within the required tolerance then no further calculations are required. However, if the error is outside the required tolerance then it is used to calculate the change in the node voltages for the next iteration, as described by equation (14).

$$[V_{new}] = [V_{old}] + inv([J]) \left[Err \right] \tag{14}$$

[J] is the Jacobian matrix and can defined in its general form for a DC system by equation (15) [30].

$$[J] = \left[\frac{\partial P}{\partial V}\right] \tag{15}$$

The Jacobian matrix only considers the change in the target injected powers due to the change in unknown voltages. The node which is operating as a slack bus is therefore not considered since its node voltage is known and its injected power is not. The Jacobian matrix is therefore a n-1 square matrix and its elements can be calculated using equations (16) and (17).

$$\frac{\partial P_i}{\partial V_i} = 2Y_{ii}V_i + \sum_{j=1, j\neq i}^{n} Y_{ij}V_j \tag{16}$$

$$\frac{\partial P_i}{\partial V_j} = V_i Y_{ij} \tag{17}$$

Hence, using the example system shown in Figure 9 and selecting node 1 as the DC slack bus, the Jacobian matrix can be given by equation (18).

$$[J] = \begin{bmatrix} \frac{\partial P_2}{\partial V_2} & \frac{\partial P_2}{\partial V_3} \\ \frac{\partial P_3}{\partial V_2} & \frac{\partial P_3}{\partial V_3} \end{bmatrix} = \begin{bmatrix} Y_{21}V_1 + 2Y_{22}V_2 + Y_{23}V_3 & Y_{23}V_2 \\ Y_{32}V_3 & Y_{31}V_1 + Y_{32}V_2 + 2Y_{33}V_3 \end{bmatrix} \tag{18}$$

Equation (11) is based on the assumption that there are no shunt losses in the DC grid. The shunt losses in a grid will normally be very small and hence little error is introduced by assuming that they are zero. However, for grids where the shunt losses are relatively high, the error in the power flow calculation can be significant. By assuming that the shunt conductance can be lumped together and split equally at each end of the cables, equation (11) can be modified to equation (19).

$$[P_i] = [V_i].\times\left([Y_{ij}][V_j] + [V_i].\times[Y_{shunt-i}]\right) \tag{19}$$

Equation (19) is used for the power solver in this work because it is more accurate than equation (11) as shown in Appendix B.

A Power Flow Solver has been developed in MATLAB with a PSCAD interface for the NAWC model. The main function of the PFS is to calculate the required DC voltage orders in order to obtain the desired DC power for each of the onshore converters without exceeding the system's nominal operating limits.

The key steps for the PFS are as described below and a flow chart is presented in Figure 10:

1. The user enters the DC system data directly into the MATLAB file. The DC system data includes the admittance values for each cable, the converter power rating, the nominal DC voltage limits and the cable current limits.
2. Using the PSCAD GUI, the user enters the target DC voltage for the first onshore VSC and the target DC power values for the other onshore converters. The user also selects if the PFS should be run automatically at a specific frequency or manually.
3. The algorithm checks that the power required by the grid is within the slack bus's capability. If it is not an error code 1 is generated and the program stops.
4. PSCAD passes the user input data and the DC power values for each of the windfarms to the MATLAB file.
5. The power flow is initially calculated based on the assumption that all node voltages are equal to the slack bus node voltage (MMC1).
6. If the error is greater than the required error, then the Jacobian matrix is solved, the node voltages are updated and the powers at each node are recalculated. This step is repeated until the error is within the required tolerance.
7. The node power, voltages and cable currents are checked to make sure that they are within nominal operating frame for the system.
8. Providing none of the system operating limits have been violated, MATLAB sends the calculated DC power and voltages to PSCAD. However, if any of limits have been exceeded, then MATLAB sends the previous DC power and voltages to PSCAD. MATLAB also sends an error code to PSCAD, so that the user can identify which limit has been breached. Error code 2,3 and 4 are generated for a power overload, DC voltage violation and cable current overload respectively.

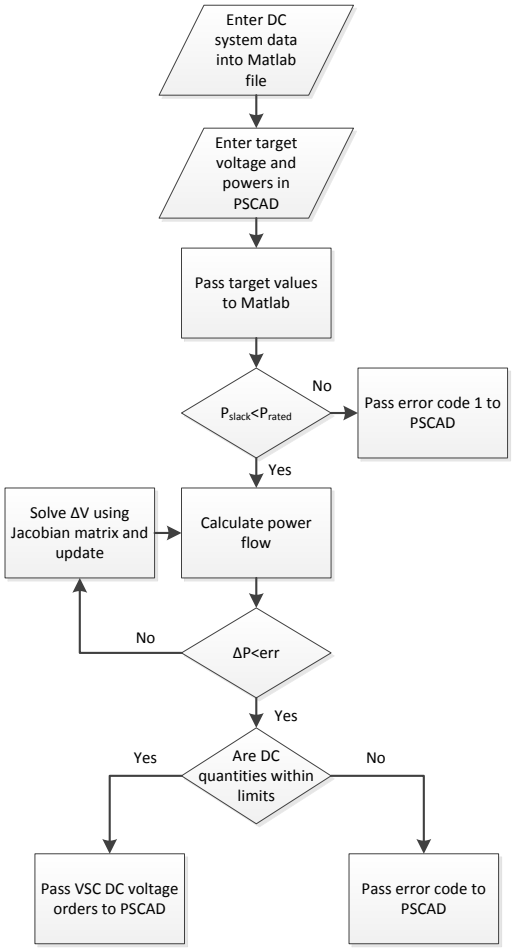

Figure 10: Flow chart for power flow solver

4.2 Overview of VSC Controls

For a VSC-HVDC scheme which connects two active networks, one converter controls active power or frequency and the other converter controls the DC link voltage. The converters at each end of the link are capable of controlling reactive power or the AC voltage at the Point of Common Coupling (PCC). For a point-to-point VSC-HVDC link which is employed for the connection of an offshore windfarm, the offshore MMC's function is to regulate the offshore AC network's voltage and frequency [32] and the onshore MMC's function is to regulate the DC voltage. In a MTDC network, such as the one shown in Figure 2, the offshore converters can be controlled in the same way as they are in a point-to-point link. The regulation of the DC link voltage for a MTDC system is however more complex than in a point-to-point link.

Figure 11 shows the different ways a typical VSC controller can be configured depending upon the type of AC network the VSC is connected to (traditional onshore AC network or a weak offshore AC network) and the type of control employed.

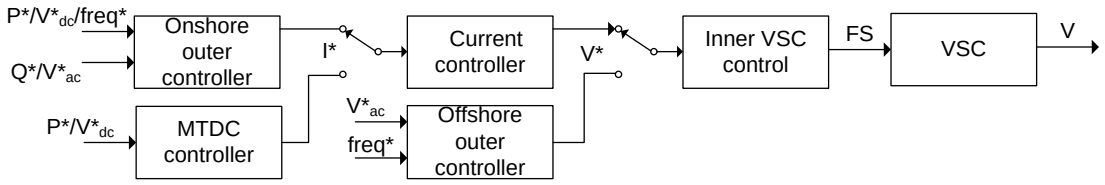

Figure 11: MMC control system basic overview

The internal VSC controls for an MMC typically include a modulation controller, a Capacitor Balancing Controller (CBC) and a Circulating Current Suppressing Controller (CCSC). These controls are specific to the converter topology and are therefore not modelled in this work.

4.2.1 Current controller

Unlike the internal MMC controls, the current controller, outer controllers and MTDC controllers are generally not VSC topology specific. The current controller is typically a fast feedback controller, which produces a voltage reference for the MMC based upon the current set-point from the outer feedback controller. Positive sequence dq control, which is commonly used for VSCs is employed for the MMC in this work because it can limit the phase currents under balanced operating conditions and can provide a faster response than direct control of the voltage magnitude and phase.

The impedance between the internal converter voltage, V_{ca}, and the AC system voltage, V_{sa}, for phase A is shown in Figure 12. The phase shift and change in voltage magnitude introduced by the converter transformer, is accounted for in the implementation of the controller as shown in Figure 19, and it is therefore not discussed in this analysis.

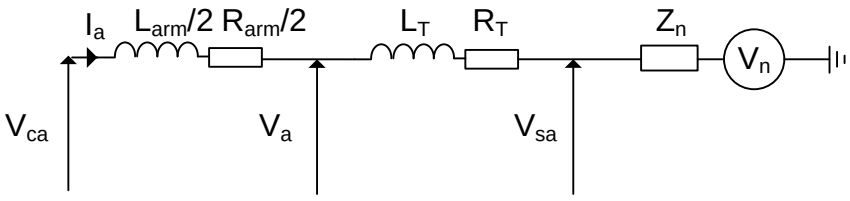

Figure 12: MMC phase A connection to AC system

Equation (20) describes the relationship between the internal converter voltage and the AC system voltage for phase A.

$$V_{ca} - V_{sa} = \left(\frac{L_{arm}}{2} + L_T\right)\frac{dI_a}{dt} + \left(\frac{R_{arm}}{2} + R_T\right)I_a \qquad (20)$$

Equation (20) can be reduced to (21).

$$V_{csa} = L\frac{dI_a}{dt} + RI_a \tag{21}$$

where:

$$V_{csa} = V_{ca} - V_{sa} \qquad L = \frac{L_{arm}}{2} + L_T \qquad R = \frac{R_{arm}}{2} + R_T \tag{22}$$

For the three-phases:

$$\begin{pmatrix} V_{csa} \\ V_{csb} \\ V_{csc} \end{pmatrix} = (R + pL)\begin{pmatrix} I_a \\ I_b \\ I_c \end{pmatrix} \tag{23}$$

In the dq synchronous reference frame equation (23) becomes equation (24).

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = R\begin{bmatrix} I_d \\ I_q \end{bmatrix} + Lp\begin{bmatrix} I_d \\ I_q \end{bmatrix} + \omega L\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}\begin{bmatrix} I_d \\ I_q \end{bmatrix} \tag{24}$$

Where $\begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}$ is the matrix representation of the imaginary unit j.

Expanding equation (24) and noting that $V_d = V_{cd} - V_{sd}$ and $V_q = V_{cq} - V_{sq}$, equations (25) and (26) are produced.

$$V_{cd} - V_{sd} = RI_d + LpI_d - \omega LI_q \tag{25}$$

$$V_{cq} - V_{sq} = RI_q + LpI_q + \omega LI_d \tag{26}$$

The equivalent circuit diagrams for the plant in the dq reference frame are given in Figure 13.

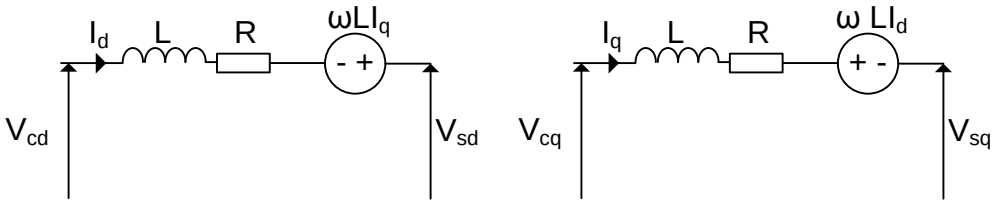

Figure 13: Equivalent dq circuit diagrams

Applying the Laplace transform with zero initial conditions to equations (25) and (26) gives equations (27) and (28).

$$V_{cd}(s) - V_{sd}(s) = RI_d(s) + LsI_d(s) - \omega LI_q(s) \tag{27}$$

$$V_{cq}(s) - V_{sq}(s) = RI_q(s) + LsI_q(s) + \omega LI_d(s) \tag{28}$$

The plant equations in the Laplace domain can be represented by state-block diagrams, with the (s) notation neglected, as shown in Figure 14.

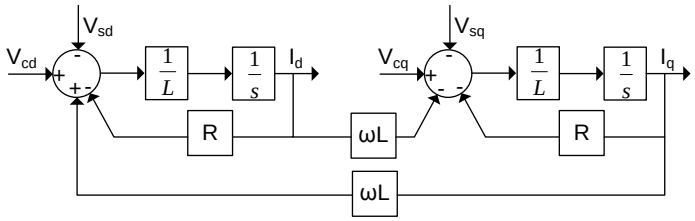

Figure 14: State-block diagram for system plant in dq reference frame

The state-block diagram in Figure 14 clearly shows that there is cross-coupling between the d and q components. The effect of the cross-coupling can be reduced by introducing feedback nulling, which effectively decouples the d and q components as shown in Figure 15.

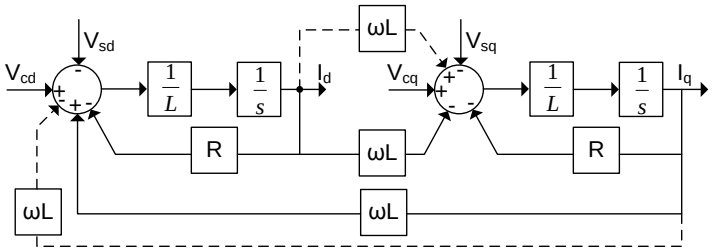

Figure 15: State-block diagram with feedback nulling

The d and q currents are controlled using a feedback PI controller as shown in Figure 16. The d and q components of the system voltage (V_{sd} and V_{sq}) act as a disturbance to the controller. The effect of this disturbance is mitigated through the use of feed-forward nulling, highlighted in Figure 15. The MMC is represented as a unity gain block (i.e. $V_{cd}^*=V_{cd}$), which is representative of its operation providing that the converter has a high level of accuracy with a significantly higher bandwidth than the current controller. The d-axis current control loop in Figure 16 can be simplified to Figure 17, due to the cancellation of the disturbance term. This is equally applicable to the q-axis.

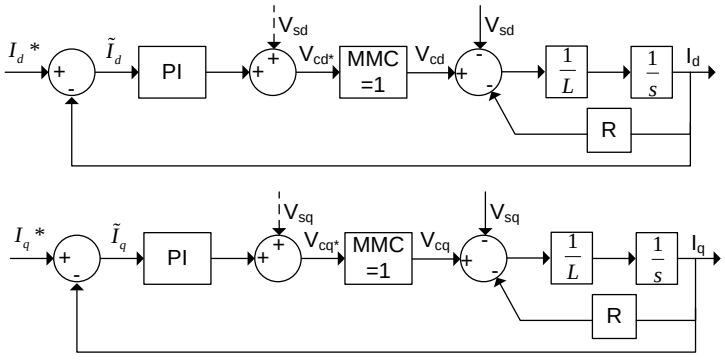

Figure 16: Decoupled d and q current control loops

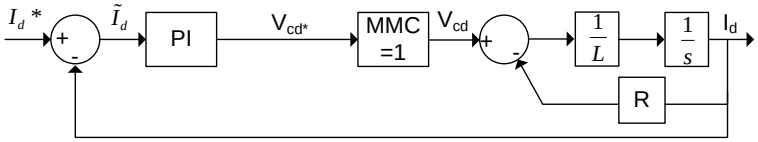

Figure 17: d-axis current loop without d-axis system voltage disturbance

Using Mason's rule the plant representation is simplified to a single block as shown in Figure 18.

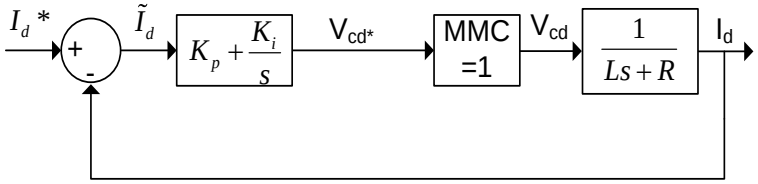

Figure 18: Simplified d-axis current control loop

The transfer function for the control loop can be calculated as follows [33]:

$$\frac{I_d}{I_d*} = \frac{\frac{1}{s}\left(K_i + K_p s\right)\left(\frac{1}{Ls+R}\right)}{1+\frac{1}{s}\left(K_i + K_p s\right)\left(\frac{1}{Ls+R}\right)\times 1} \tag{29}$$

The closed loop transfer function can be reduced to a first order transfer function which allows the PI controller to be tuned for a specific bandwidth, BW, with a critically damped response [33, 34]. Equation (29) can be reduced to a first order transfer function as follows:

$$\frac{I_d}{I_d*} = \frac{\frac{K_p}{s}\left(s+\frac{K_i}{K_p}\right)\frac{1}{L\left(s+\frac{R}{L}\right)}}{1+\frac{K_p}{s}\left(s+\frac{K_i}{K_p}\right)\frac{1}{L\left(s+\frac{R}{L}\right)}} \tag{30}$$

By selecting $\frac{K_i}{K_p} = \frac{R}{L}$ equation (30) is reduced to equation (31)

$$\frac{I_d}{I_d*} = \frac{\frac{K_p}{sL}}{1+\frac{K_p}{sL}} = \frac{K_p}{sL+K_p} = \frac{1}{s\frac{L}{K_p}+1} \tag{31}$$

The full closed loop transfer function is therefore reduced to a first order transfer function with a time constant $\tau_{ic} = L/K_p$. The bandwidth in radians for a first order system is equal

to $1/\tau_{ic}$. Hence equation (31) can be re-written as equation (32), where BW_{ic} is the inner controller bandwidth.

$$G_{CL} = \frac{1}{\frac{s}{BW_{ic}} + 1} \tag{32}$$

The proportional gain, K_p , and integral gain, K_i , can be calculated for given values of L, R and BW from equations (33) and (34) respectively.

$$K_p = BW_{ic} \times L \tag{33}$$

$$K_i = \frac{R}{L} K_p = BW_{ic} \times R \tag{34}$$

The advantage of this method, as opposed to simplifying the transfer function to that of a classic 2nd order system, is that the exact bandwidth for the control loop can be selected through a very simple tuning process. Also a phase margin of 90° with an infinite gain margin is assured. The disadvantage is that since only the bandwidth can be selected, there is less flexibility when optimising the controller to meet set performance criteria.

The performance criteria for the inner current loop are that it is fast, stable and has no overshoot. Tuning the PI controller to provide sufficient bandwidth using the first order transfer function is therefore a suitable approach. A bandwidth of 320Hz was found to offer good performance.

The block diagram for the implementation of the current controller is shown in Figure 19. The phase voltages and currents, measured at the PCC are scaled, and the output converter voltage set-points are advanced 30° to compensate for the transformer. The d-axis and q-axis current orders from the outer controller have limits to prevent valve overcurrents under balanced conditions.

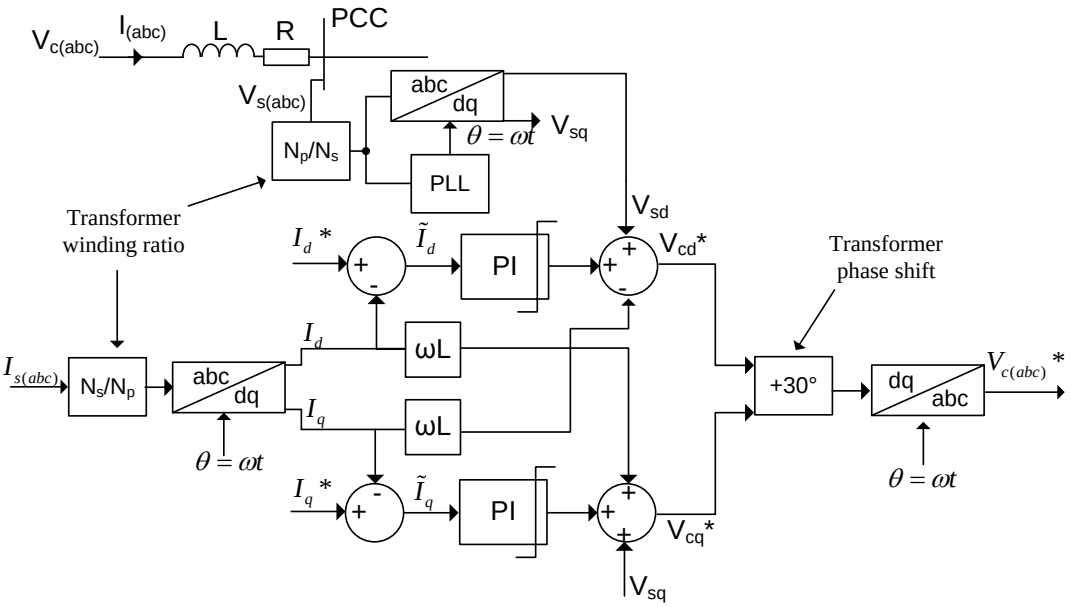

Figure 19: dq current controller implementation

4.2.2 Active and reactive power controllers

In the magnitude invariant dq synchronous reference frame, the power flow at the PCC can be described by equations (35) to (37).

$$S_{dq} = \frac{3}{2} V_{dq} I_{dq}{}^{*} = \frac{3}{2}(V_{sd} + jV_{sq})(I_d - jI_q) \tag{35}$$

$$P = \frac{3}{2}\left(V_{sd} I_d + V_{sq} I_q\right) \tag{36}$$

$$Q = \frac{3}{2}\left(V_{sq} I_d - V_{sd} I_q\right) \tag{37}$$

The q-axis is aligned with V_a such that $V_{sq} = 0$. Equations (36) and (37) are therefore reduced to equations (38) and (39).

$$P = \frac{3}{2} V_{sd} I_d \tag{38}$$

$$Q = -\frac{3}{2} V_{sd} I_q \tag{39}$$

Equations (38) and (39) show that the active power is controlled by I_d and the reactive power is controlled by I_q. The I_d and I_q references to the current controller are set using feedback PI controllers. The K_p and K_i values for the controllers can be calculated according to equations (40) and (41), where BW_p is the bandwidth of the power controller.

$$K_p = \frac{BW_p}{1.5 V_{sd} BW_{ic}} \tag{40}$$

$$K_i = BW_{ic} K_p \tag{41}$$

V_{sd} is the value of d-axis voltage at the PCC, which has a nominal value in this model of 300kV. Providing that the AC system is relatively strong this value is effectively fixed, and therefore the PI controller parameters can be calculated based on the nominal value for V_{sd}. In any case, a variation in V_{sd} produces a proportional change in the power controller bandwidth; hence a relatively large variation in V_{sd} of 10% produces only a 10% change in BW_p. Note that the relationship $\frac{K_i}{K_p} = \frac{1}{\tau_{ic}}$ is ensured irrespective of V_{sd}. Feedback PI controllers are employed to give the I_d and I_q set-points to the inner current controllers based on the active and reactive power orders respectively.

The active and reactive power demands for a VSC-HVDC converter are typically ramped at 1GW/min under normal operating conditions and at 1GW/s for emergency power control[1]. The outer power loop does not therefore require a large bandwidth and hence a bandwidth of 30Hz is more than sufficient.

4.2.3 DC voltage controller

MMCs, unlike two-level VSCs, do not normally employ DC side capacitor banks and therefore the MMC's equivalent capacitance, C_{eq}, is used in the DC side plant model shown in Figure 21. The equivalent capacitor value based on the total stored energy in the MMC is calculated according to equation (42). However, during normal operation only half of the MMC's capacitors are in-circuit and therefore the equivalent MMC capacitance is given by equation (43).

$$C_{eq} = \frac{6C_{sm}}{N} \tag{42}$$

$$C_{eq} = \frac{3C_{sm}}{N} \tag{43}$$

In the following test case, the DC voltage step response for a MMC Detailed Equivalent Model (DEM) is compared with the Standard AVM (SAVM) when employing a 230µF capacitor (eq (42)) and a 115µF (eq (43)) capacitor. Figure 20 shows that the initial response of the SAVM with a 115µF capacitor is more accurate than the SAVM with a 230µF capacitor. However, after the initial response the SAVM with a 230µF capacitor is more accurate.

[1] Based on discussions with a HVDC controls expert from a leading HVDC manufacturer.

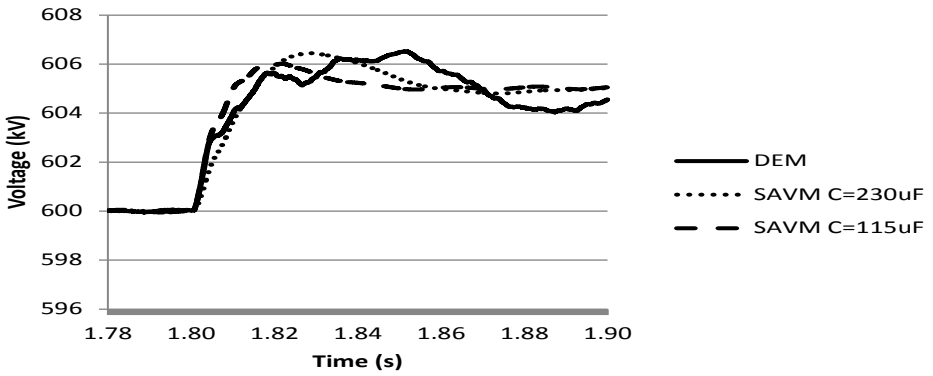

Figure 20: The models' DC voltage response to a 5kV step change in the DC voltage controller reference voltage at 1.8s.

This result indicates that the faster DC dynamics can be modelled more accurately using a capacitance value based on the MMC's in-circuit capacitance, while the slower dynamics can be modelled more accurately using a capacitance value based on the MMC's total stored energy. The overall DC dynamics for an MMC can therefore not be modelled using a single value fixed capacitor. The user must therefore select the equivalent capacitance value with care. In this work, a capacitance value based on the MMC's total stored energy is considered to be more appropriate.

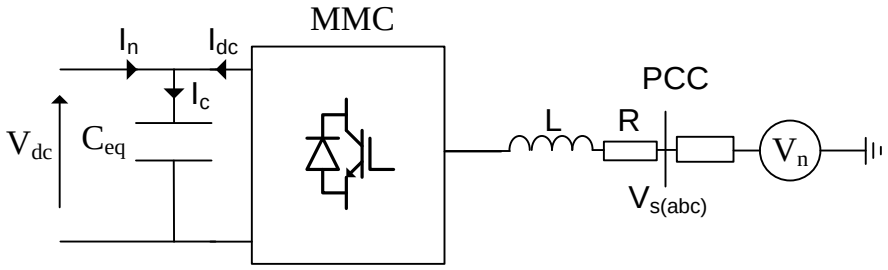

Figure 21: DC side plant

With reference to Figure 21 the DC link voltage can be described by equation (44) and the power balance between the AC and DC system can be described by equation (45), assuming no converter losses.

$$C_{eq}\frac{dV_{dc}}{dt} = I_n + I_{dc} \tag{44}$$

$$I_{dc}V_{dc} = 1.5V_{sd}I_{sd} \tag{45}$$

Hence:

$$\frac{dV_{dc}}{dt} = \frac{I_n}{C_{eq}} + \frac{3V_{sd}I_{sd}}{2C_{eq}V_{dc}} \tag{46}$$

Taking partial derivatives gives equation (47), where the subscript 'o' denotes operating point:

$$\frac{d\Delta V_{dc}}{dt} = \frac{1}{C_{eq}}\Delta I_n - \frac{3V_{sdo}I_{sdo}}{2C_{eq}V_{dco}^{\ 2}}\Delta V_{dc} + \frac{3V_{sdo}}{2C_{eq}V_{dco}}\Delta I_{sd} \tag{47}$$

$$C_{eq}\frac{d\Delta V_{dc}}{dt} = \Delta I_n - 1.5K_V K_G \Delta V_{dc} + 1.5K_V \Delta I_{sd} \tag{48}$$

where:

$$K_V = \frac{V_{sdo}}{V_{dco}} \qquad K_G = \frac{I_{sdo}}{V_{dco}} \tag{49}$$

The State Feedback System Block diagram (SFSB) for the DC voltage control loop is shown in Figure 22.

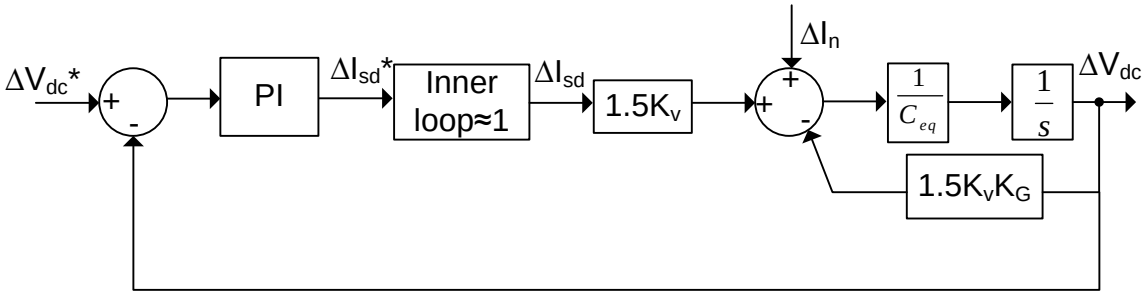

Figure 22: SFSB for DC voltage control loop

The transfer function for the control loop can be derived as follows:

$$\frac{\Delta V_{dc}}{\Delta V_{dc}*} = \frac{\frac{1.5K_V}{s}(sK_p + K_i)}{C_{eq}s + 1.5K_V K_G + \frac{1.5K_V}{s}(sK_p + K_i)} \tag{50}$$

$$\frac{\Delta V_{dc}}{\Delta V_{dc}*} = \frac{1.5K_V(sK_p + K_i)}{C_{eq}s^2 + 1.5K_V(K_G + K_p)s + 1.5K_v K_i} \tag{51}$$

Typically $K_G << K_p$ and hence equation (51) can be reduced to equation (52):

$$\frac{\Delta V_{dc}}{\Delta V_{dc}*} = \frac{1.5K_V(sK_p + K_i)}{C_{eq}s^2 + (1.5K_V K_p)s + 1.5K_v K_i} \tag{52}$$

The key performance criteria for the DC voltage outer controller are that it is stable, with excellent steady-state tracking and good disturbance rejection.

The outer DC link voltage loop is tuned assuming that the inner current loop is a unity gain block. This is a valid assumption providing that the outer loop is significantly slower than the inner current loop. The maximum available bandwidth for the outer controller is

therefore limited to one order of magnitude smaller (≈30Hz) than the inner current loop bandwidth (=320Hz). The controller's ability to reject disturbances, particularly low frequency disturbances, improves with bandwidth due to the increase in integral gain. Tuning the outer loop controller for a bandwidth of 20Hz (point at which the gain of equation (52) is -3dBs) and using a damping ratio of 0.7 was found to offer a good level of performance.

4.2.4 MTDC Control

A review of MTDC control methods is given in [35, 36]. Generally speaking these methods can be categorised as centralised DC slack bus, voltage margin control, droop control or a combination of the aforementioned control methods. Typical DC voltage/current characteristics for a converter employing the different MT control methods are shown in Figure 23.

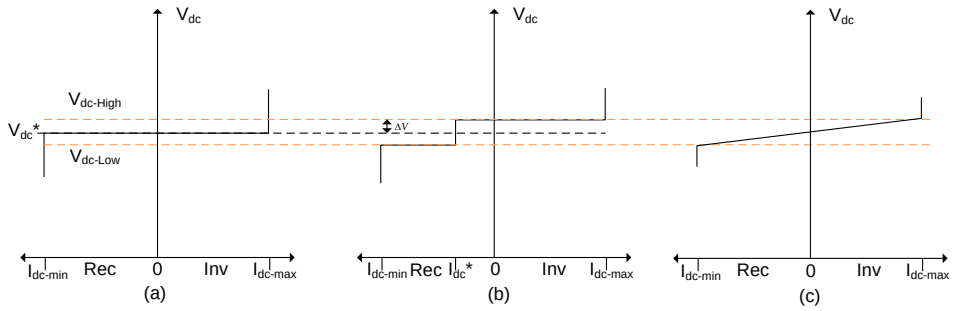

Figure 23: Typical MT control DC voltage/current characteristics: (a) slack bus; (b) voltage margin; (c) droop

Employing a centralised DC slack bus means that one of converters operates in DC voltage control and must import/export the necessary active power in order to regulate the DC voltage. However, if the required active power is outside of the DC slack bus converter's capability then it will no longer be able to control the DC voltage, resulting in grid instability. An alternative is to operate another converter in voltage margin control. The converter employing voltage margin control operates as a constant power controller and transitions to DC voltage control if the DC voltage violates pre-set limits. Voltage margin control therefore improves the reliability of the system in comparison to a centralised DC slack bus. There are however a number of limitations when employing voltage margin control, such as the inability of more than one converter to participate in DC voltage regulation simultaneously.

In droop control more than one converter is able to participate in regulating the DC voltage and therefore the burden of continuously balancing the system's power flow is not placed

upon a single converter. There are many types of droop controller, however they all work on the principle of modifying the converter's active power flow in order to regulate the DC voltage in accordance to their droop characteristic. The gradient of the droop slope determines the converter's response to a change in the DC voltage/current. The converter operates in current limit mode when the DC voltage thresholds are reached.

The droop controller used for this work is referred to as the Autonomous Converter Controller (ACC) which was originally proposed by Alstom Grid [1]. The implementation of ACC for this work is shown in Figure 24 and Figure 25.

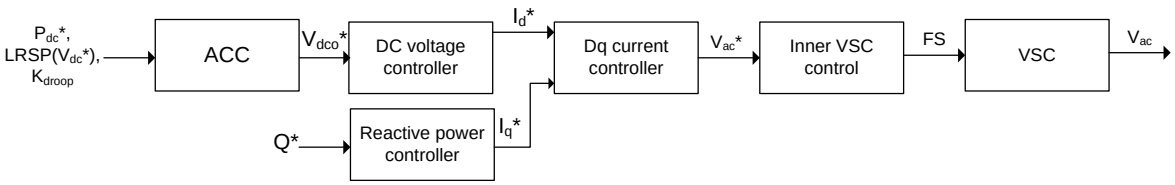

Figure 24: Basic VSC control structure for ACC

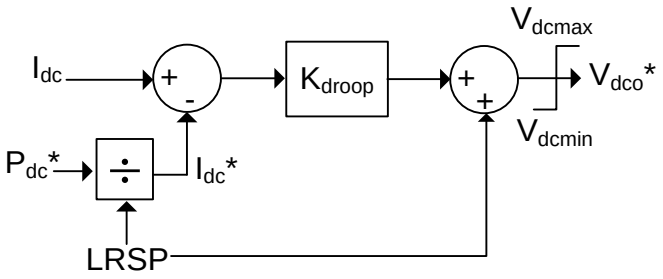

Figure 25: ACC implementation

The controller receives the DC power order, the Load Reference Set-Point (LRSP) and the droop gain from the PFS. It should be noted that the LRSP is the same as the target DC voltage. The term LRSP is used in this report as it is in keeping with the original literature on the ACC. At steady-state, I_{dc} will be equal to I_{dc}* providing that the PFS is accurate, and hence the voltage order sent to the DC voltage controller, V_{dco}*, is equal to the LRSP. However, during transients, V_{dco}* varies in accordance to the droop characteristic ((I_{dc}-I_{dc}*)K_{droop}). The setting of the droop gain is discussed in section 5.

4.2.5 Control System for VSC Connected to a Windfarm

In situations where the VSC is connected to an islanded or very weak network, the VSC's function is to regulate the AC network's voltage and frequency [32]. In this mode of operation, the VSC absorbs all of the power generated by the offshore windfarm. The AC voltage magnitude and frequency for the offshore network can be controlled with or without an inner current loop [32, 37]. In this work, the voltage magnitude is set by

controlling the d-axis voltage without an inner current loop and by using a voltage controlled oscillator to set the angle based on the frequency set-point for the offshore network as shown in Figure 26. This approach was found to offer good stability, however it should be noted that the arm currents cannot be limited for an offshore AC network fault without supplementary control.

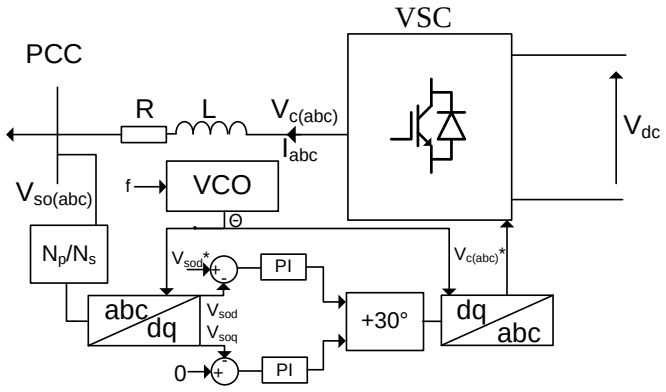

Figure 26: Implementation of the AC voltage controller for the offshore network

4.3 Windfarm Control

A 1GW offshore windfarm would typically contain 200 wind turbines based on a 5MW turbine design. The wind turbines are typically connected to two 500MW AC collector stations where the voltage is increased from 33kV to 220kV for transmission to the offshore converter. A range of modelling approaches exists for windfarms [38-40]. Modelling such a large number of wind turbines in detail in EMT simulation packages is very computationally intensive and unnecessary for some VSC-HVDC studies. Simplified windfarm models are therefore often employed [32]. For this work a simple windfarm model consisting of a three phase voltage connected to a 33kV/220kV transformer is employed since the HVDC link is the focus.

A simplified diagram for the offshore windfarm control system is shown in Figure 27 and Figure 28.

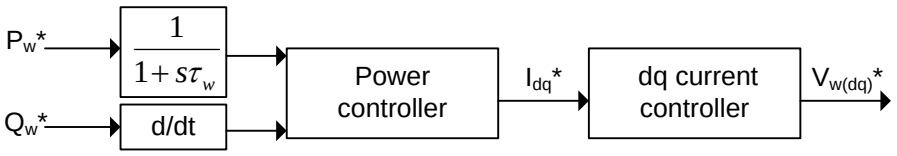

Figure 27: Block diagram for the windfarm power controller

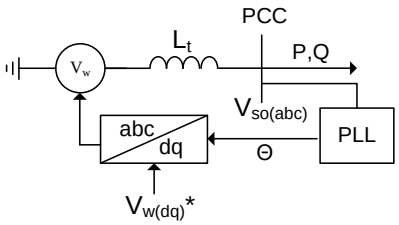

Figure 28: Implementation of the windfarm power controller

The wind turbine, generator and back-to-back converter are represented as a first order transfer function with a time constant, τ_w. The natural time constants, τ_o, for three commercial wind turbines have been calculated in [41] and are presented in Table 3.

P_{rated} (MW)	υ_{rated} (m/s)	τ_o (s)
1.5	13	16.4
2.5	12.5	22.6
3.6	14	25.8

Table 3: Calculated time constants for commercial wind turbines modified from [41]

Extrapolating the data given in Table 3 for a 5MW wind turbine gives a natural time constant of approximately 30s. Small signal analysis carried out in [41] has shown that the actual wind turbine time constant, τ, varies with wind speed, v, and can be described by equation (53).

$$\tau = \tau_o \times \frac{v_{rated}}{v} \tag{53}$$

The maximum cut out speed for a large commercial wind turbine is typical 25 m/s with a rated wind speed of 12-14 m/s [42, 43]; hence the smallest time constant for a typical 5MW wind turbine is approximately 15s. Setting the windfarm first order transfer function time constant, τ_w, to 15s would require very lengthy simulation times and therefore it is reduced to 0.15s which is suitable for this model.

The windfarm reactive power order to the power controller is limited to a rate of change of 1MVAr/ms. The structure of the power controller and the current controller employed for the windfarm are effectively the same as for the MMC and are therefore not repeated here. The power controller and current controller are tuned using the first order transfer function to give a bandwidth of 10Hz and 100Hz respectively. The power controller time constant is therefore approximately one order of magnitude smaller than the reduced windfarm time constant.

5 Operating frame

The operating frame of the system defines amongst other parameters, the DC voltage and DC current limits in the system at steady-state and for transient events. During normal operation, it is the PFS responsibility to ensure that the nominal operating frame is not breached. However, for fast transient events the PFS has no effective control over the system. In this case, the system's DC voltages and currents are predominantly determined by the system configuration, system parameters, initial operating conditions, and converter controls.

The maximum DC voltage and current values due to transient events are defined by the dynamic operating frame. The dynamic operating frame has two levels; the first defines the maximum DC voltage and current values which the system can be subjected to for a pre-determined period of time and the second defines the maximum instantaneous DC voltage and current values. The pre-determined period of time is dependent upon how quickly the PFS can regain control of the system to bring the DC current and voltage values to within the nominal operating frame. It should be noted that it is not the responsibility of the grid control system to prevent dynamic level 2 violations for some fault scenarios. For example, the DC voltage will collapse below the 0.8p.u. limit for a DC line-to-line fault.

An example of DC voltage operating frame limits is given in Table 4. The nominal limits will typically be defined by the maximum voltage drop in the system. The upper dynamic voltage limits are determined by the converters' and cables' DC voltages withstand capabilities. The lower DC voltage limit should not be set below the MMC's rectified mean DC voltage since a half bridge MMC will become uncontrollable. The impact of higher DC current values on equipment ratings and losses should also be considered when setting the lower DC voltage limits. A further refinement on using fixed limits is to employ sloped limits as proposed by Alstom Grid in [2].

Parameter	Nominal	Dynamic Level 1 (<5s)	Dynamic Level 2
Upper DC voltage limit (p.u.)	1.0	1.02	1.15
Lower DC voltage limit (p.u.)	0.96	0.9	0.8
Maximum Cable current (p.u.)	1.05	1.12	1.3

Table 4: Example operating frame limits

In order to ensure that the dynamic level 1 operating frame will not be violated, the DC voltage and current values must be known for the new operating point following the worst case transient event.

In this work, a method has been proposed to give an initial estimation of the maximum and minimum DC voltage and current operating points for the system following a severe transient event. Providing these values are within level 1 of the dynamic operating frame, the system will be able to obtain a safe operating point without the need for protective action.

The following guidelines could be used for selecting the scenario(s) which are likely to result in the highest short-term DC voltage:

1. A scenario where only one converter is able to regulate the DC voltage. This means that the burden of balancing the systems power flow is placed on a single converter resulting in the greatest deviation in the DC voltage. This could be because the other converters that are operating in ACC are blocked or are exporting maximum power.
2. The converter regulating the DC voltage has the steepest voltage/current droop characteristic. The steeper the droop, the greater the change in DC voltage for a given change in DC current.
3. Before the transient event, the converter regulating the DC voltage is importing maximum power from the AC system at the upper limit of the nominal DC voltage.
4. Consider the transient event which results in the greatest surplus of active power in the DC grid. The converter regulating the DC voltage will be forced to export the surplus of the DC power into the AC grid. The increase in the DC voltage at the converter's terminals is proportional to the change in the DC current.

In addition to guidelines 1 and 2, the following guidelines could be used for selecting the scenario(s) which are likely to result in the lowest short-term DC voltage:

5. Before the transient event, the converter regulating the DC voltage is exporting maximum power to the AC system at the lower limit of the nominal DC voltage.
6. Consider the transient event which results in the greatest deficit of active power in the DC grid. The converter regulating the DC voltage will be forced to import the deficit of the DC power from the AC grid. The decrease in the DC voltage at the converter's terminals is proportional to the change in the DC current.

Once the worst case scenarios have been identified, the new voltage and current values (after the transient event) can be calculated. In order to do this the DC voltage, DC current and droop gain before the transient event, and the DC power after the transient event for the last converter regulating the DC voltage must be known. The DC current and DC voltage after the transient event (OP2) can be calculated using equations (54) and (55) respectively. The derivation of these equations is given in the Appendix C.

$$I_{dc-op2} = \frac{\sqrt{(4 \times K_{droop} \times P_{op2} + A^2)} + A}{2 \times K_{droop}} \tag{54}$$

$$V_{dc-op2} = \left(I_{dc-op2} - I_{dc-op1}\right) \times K_{droop} + V_{dc-op1} \quad (55)$$

Where:

$$A = I_{dc-op1} \times K_{droop} - V_{dc-op1} \quad (56)$$

Equation (55) calculates the DC voltage at the terminals of the converter which is regulating the DC voltage. This DC voltage value is entered into a modified PFS along with the known DC node powers to determine the DC voltage at the other nodes. The node voltages can then be used to calculate cable currents if required.

This methodology is used in this work to determine the maximum droop gains which can be employed to ensure that the system does not exceed the dynamic level 1 limits. High droop gains for ACC (steep droop) increases the likelihood of operating frame violations and can degrade the stability of the system. However, small gains reduce the ability of the ACC to influence converter power sharing for transient events. When tuning the ACCs in this work a starting droop gain of 10 (kV/kA) is used. This gain is then reduced in an iterative fashion until there are no operating frame violations for the selected worst case scenario.

Example – ACC droop gain selection for NAWC

Based on the guidelines for selecting the scenario(s) which are likely to result in the highest DC voltage, the following scenario for the AWC system has been selected. Consider the scenario where there is no wind power on the grid, VSC2 is blocked and VSC1 is importing maximum DC power from the AC system at the upper limit of the nominal DC voltage. The operating point (OP1) for VSC1 is shown in Figure 29.

It is assumed in this scenario that up to 1400MW of wind power could be injected into the system before the PFS would have time to act[2]. The wind power is supplied by windfarm 2 (400MW) and windfarm 3 (1000MW). Since VSC3 is exporting maximum power it is unable to regulate the DC voltage. VSC1 must therefore go from importing 1000MW to exporting approximately 400MW to the AC system in order to regulate the DC voltage. The new operating point (OP2) can then be calculated for a given droop gain using equation (55). Figure 29 shows that the new operating point for VSC1, when using a

[2] In reality, it is likely that the PFS would be updated several times before the wind power on the system would change by 1400MW, but this assumption is useful for the purpose of this example.

default droop gain of 10 results in a DC voltage which is well in excess of the upper DC voltage limit.

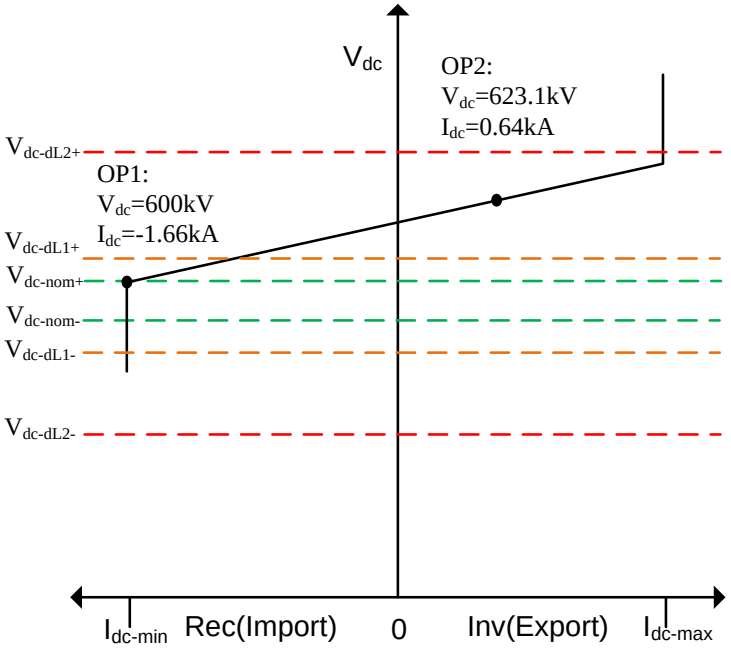

Figure 29: Operating characteristic for VSC1

An algorithm has been developed for this work in MATLAB in order to determine the maximum droop gain which can be used without operating frame violations for a given scenario. The key steps for the algorithm are described below with a simplified flow chart shown in Figure 30.

1. The user enters the DC voltage, DC current and droop gain before the transient event (OP1), and the DC power after the transient event (OP2) for the last converter regulating the DC voltage (VSC1 in this example). The user also enters the expected node powers after the transient event.
2. The algorithm calculates the DC voltage (OP2) for the last converter regulating the DC voltage using equation (55)
3. The calculated DC voltage and the estimated node powers are then used to determine the other node voltages and cable currents using the PFS.
4. The code then checks that all of the node voltages and cable currents are within the limits set by dynamic level 1. If any of the limits have been violated, the droop gain is reduced and the DC voltages and cable currents are re-calculated. This process continues until the DC voltages and cable currents are within the set limits.
5. Once the node voltages and cable currents are within the set limits, the maximum ACC gain is presented on the MATLAB console.

This algorithm determined that the maximum ACC gain should be 3.79 for the example scenario. The droop gain for this work is therefore set to 3.5. It should be noted that this algorithm is not suitable for every scenario since the user must be able to estimate the node

power at the new operating point. A diagram showing the overall control architecture and the key control layers which affect the different operating frame limits is given in Appendix D.

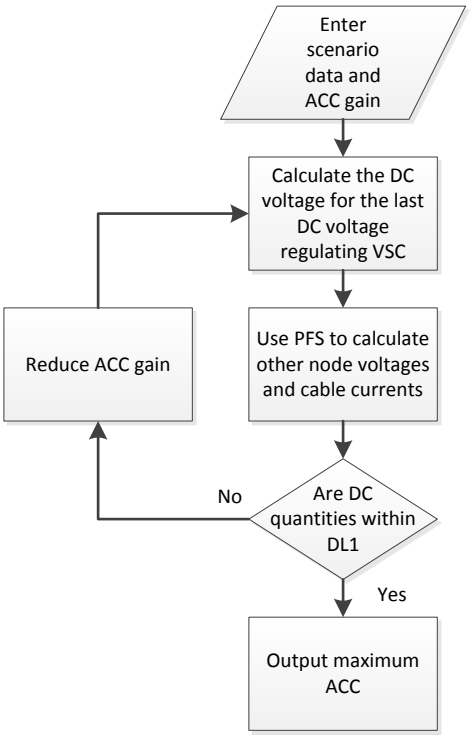

Figure 30: Flow chart for ACC gain algorithm

6 Simulation results

This section of the report presents the simulation results for the agreed case studies. Unless stated otherwise, the target DC voltage for VSC1 is 588kV and the droop gain for all ACCs is 3.5.

6.1 Steady-state error

The active power injected into the DC system by windfarm 1, P_{dc4}, windfarm 2, P_{dc5}, and windfarm 3, P_{dc6}, are approximately 500MW, 250MW and 600MW respectively. The target DC power orders for VSC2, P_{dc2}, and VSC3, P_{dc3}, are set to 600MW and 400MW respectively. The system's DC power flow at steady state is shown in Figure 31 and the accuracy of the target power flow is given in Table 5. It should be noted that only the DC power values for VSC2 and VSC3 are included in Table 5 as these are the only values which the user is able to control. This result shows that the PFS and the VSC controls are able to accurately control active power flow in steady-state.

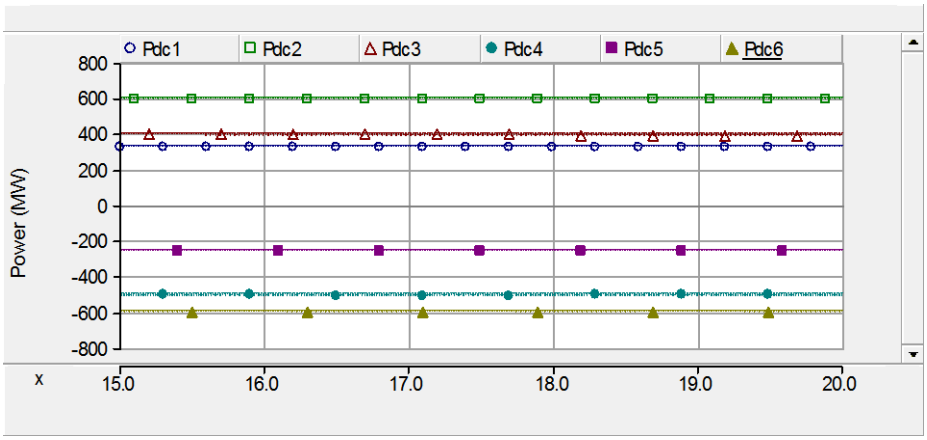

Figure 31: DC power flow at steady-state; x-axis is time in seconds

Node	Target (MW)	Simulated (MW)	Error (MW)	Error (%)
Pdc2	600	600.277	0.277	0.046
Pdc3	400	400.146	0.146	0.037

Table 5: Power flow accuracy

6.2 Droop control using same droop constants

The initial DC power and voltage orders to the converters are set to the same values as in the previous test. The droop gains for all of the converters employing ACC (1, 2 & 3) are set to 3.5 and the PFS is disabled. At 5s, the power injected by windfarm 2 increases from 250MW to 750MW using a time constant of 0.15s. Figure 32 shows that all of the converters operating in ACC regulate the DC voltage by sharing the DC power increase. The onshore converters share the increase in wind power according the systems configuration, droop gain, initial operating conditions and the point in the system where the wind power is increased.

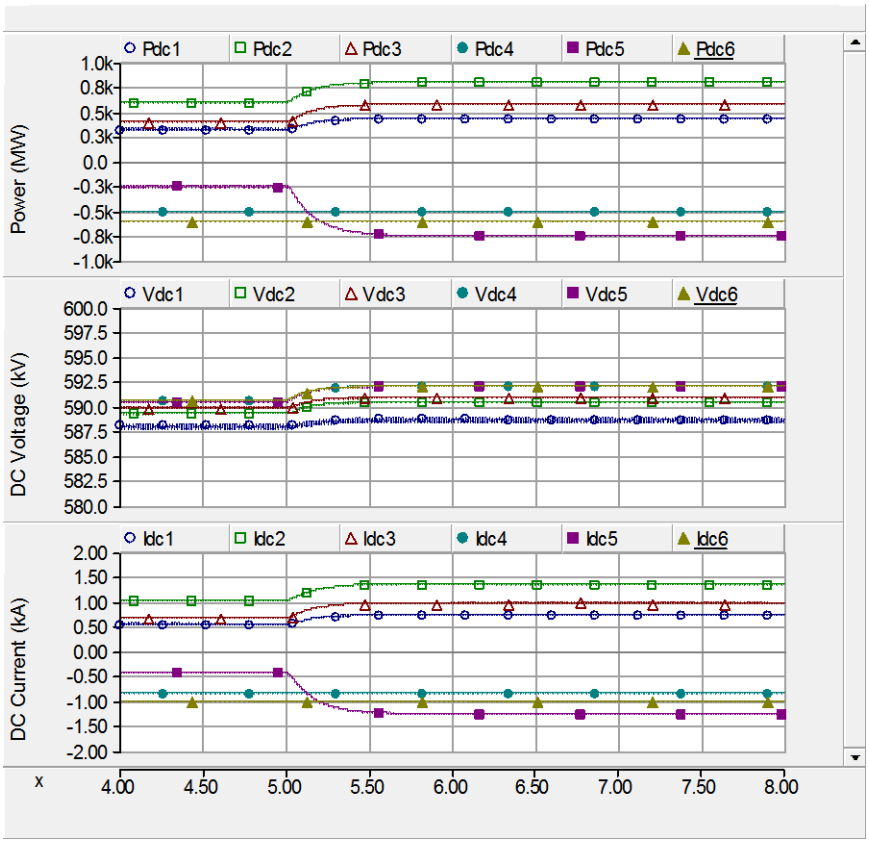

Figure 32: System's response to variations in windfarm power when employing the same droop constant; x-axis is time in seconds

6.3 Droop control using different droop constants

This scenario is the same as the previous scenario, except that the droop constant for VSC3 is reduced to 0.1. Figure 33 shows that VSC3 participates more actively in the regulation of the DC voltage as a result of reducing the droop constant.

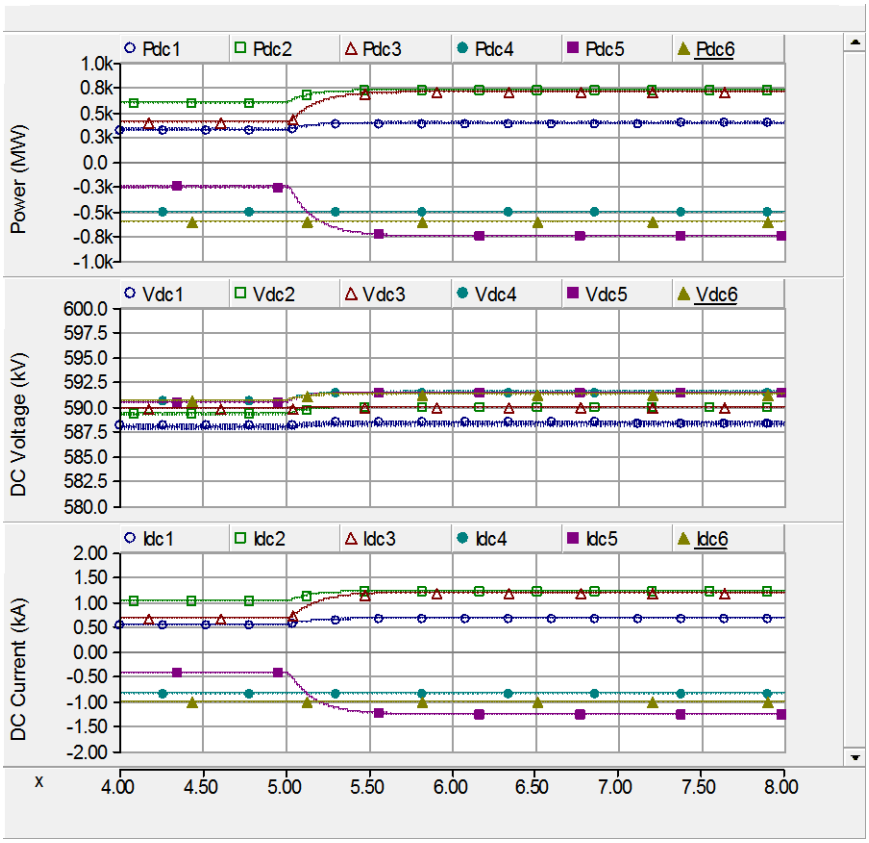

Figure 33: System's response to variations in windfarm power when employing the same droop constant; x-axis is time in seconds

6.4 Droop control using same droop constants with PFS

This scenario is the same as the scenario in section 6.2, except that the PFS is enabled with an update frequency of 10Hz. The PFS automatically adjusts the converter set-points to obtain the target DC power flows for VSC2 and VSC3 as shown in Figure 34.

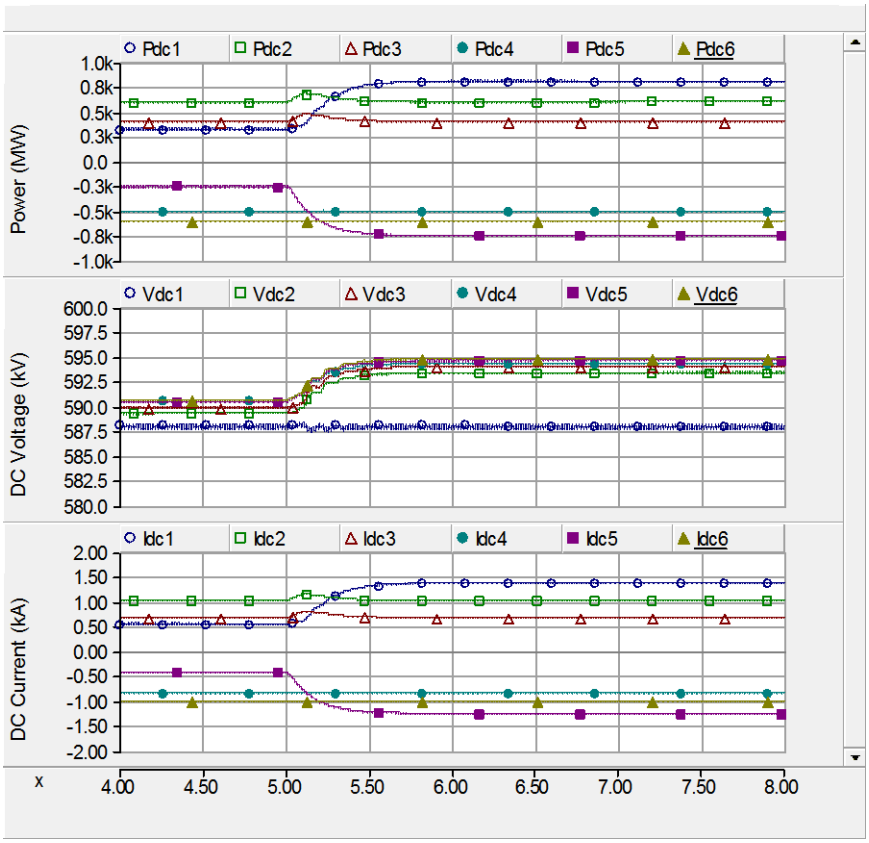

Figure 34: System's response to variations in windfarm power when employing the same droop constant with the PFS engaged using an update frequency of 10; x-axis is time in seconds.

6.5 Force power overload

The purpose of this test is to check that the PFS issues the correct error code for a DC power overload. In order to do this, the power order for VSC2 is decreased from 600MW to -100MW at 4s. The next time the PFS is updated (4.1s), it issues error code 1, which means that the PFS can no longer ensure that VSC2 and VSC3 can obtain their target DC power values as this would overload VSC1. Hence, the PFS does not issue any set-point changes to the converters.

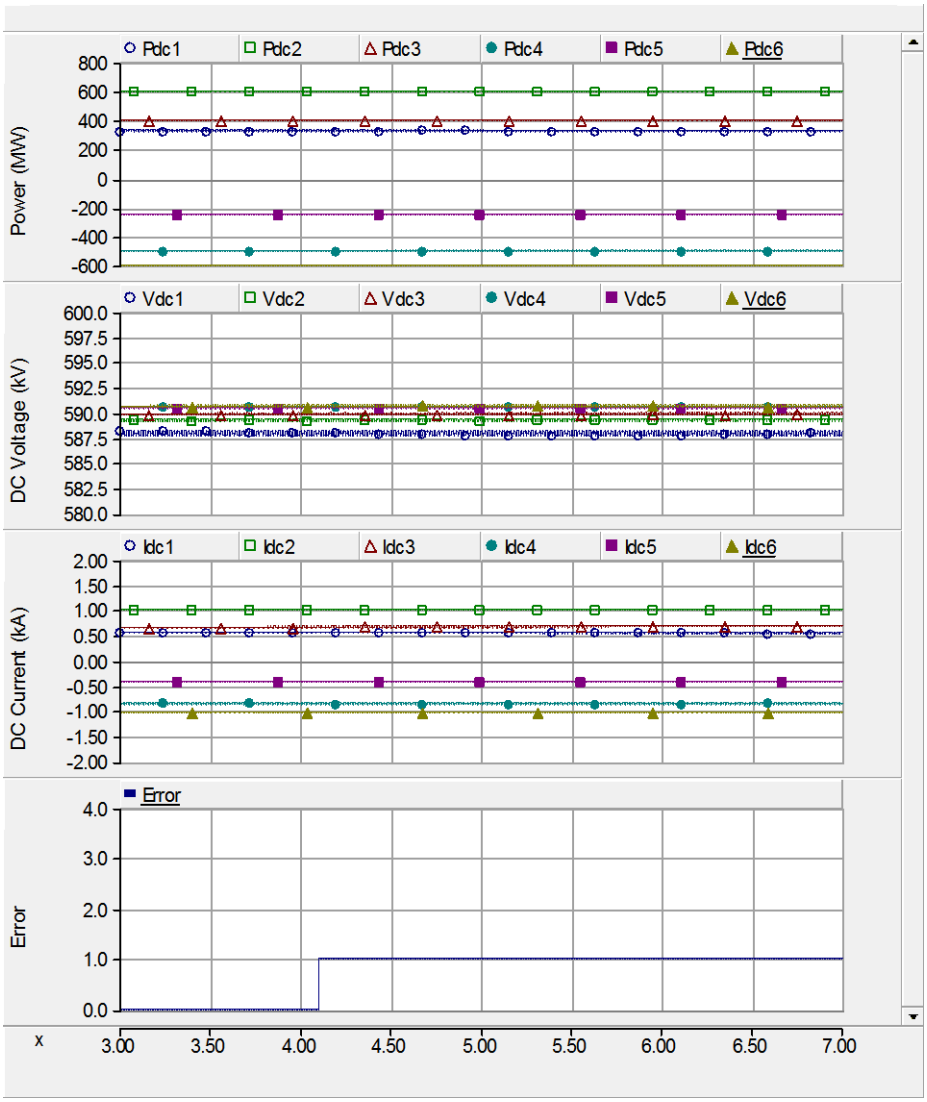

Figure 35: System's response to a DC power overload; x-axis is time in seconds.

6.6 Force DC voltage overload

The purpose of this test is to check that the PFS issues the correct error code for a DC voltage overload. In order to do this, the target DC voltage for VSC1 is increased from 588kV to 598kV at about 4s. The PFS checks the new target voltage at 4.1s and re-solves the power flow. Due to the increase in the target voltage for VSC1, one of the other nodes would exceed its upper voltage limit of 600kV, if the new converter orders were issued. The PFS therefore maintains the previous converter orders and issues error code 3 as shown in Figure 36. Error code 3 informs the user that the solved DC voltages are out of the limits imposed by steady-state operating frame.

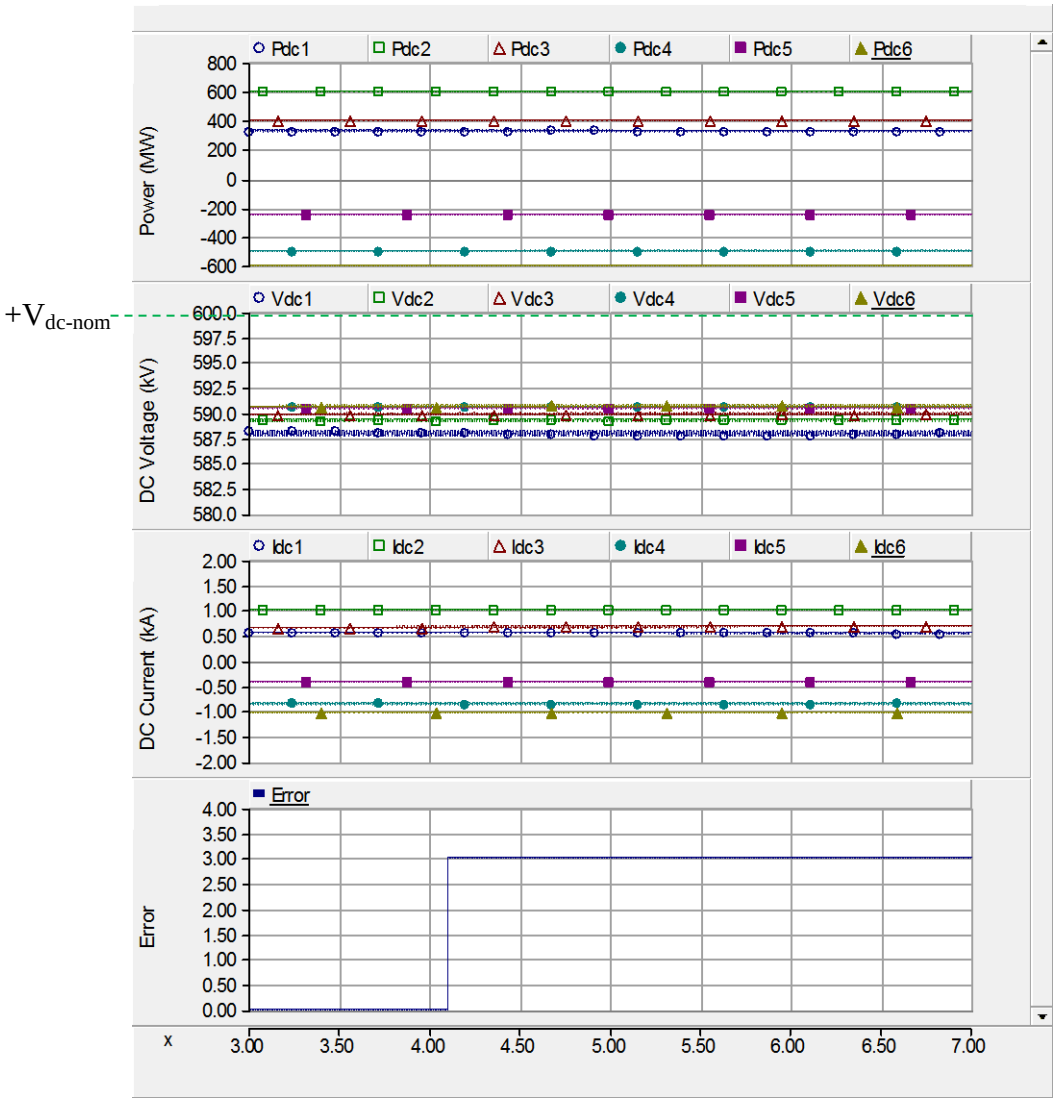

Figure 36: System's response to a DC voltage overload; x-axis is time in seconds.

6.7 Force DC cable current overload

In this scenario, the cable current rating for the cable connected between VSC2 and VSC5 (cable25) was reduced to 1.1kA from the nominal rating of 1.75kA. At 4s the power order for VSC2 is increased from 600MW to 700MW. The PFS issues error code 4 as shown in Figure 37, which indicates that the PFS cannot operate VSC2 at 700MW without exceeding the current rating for cable 25.

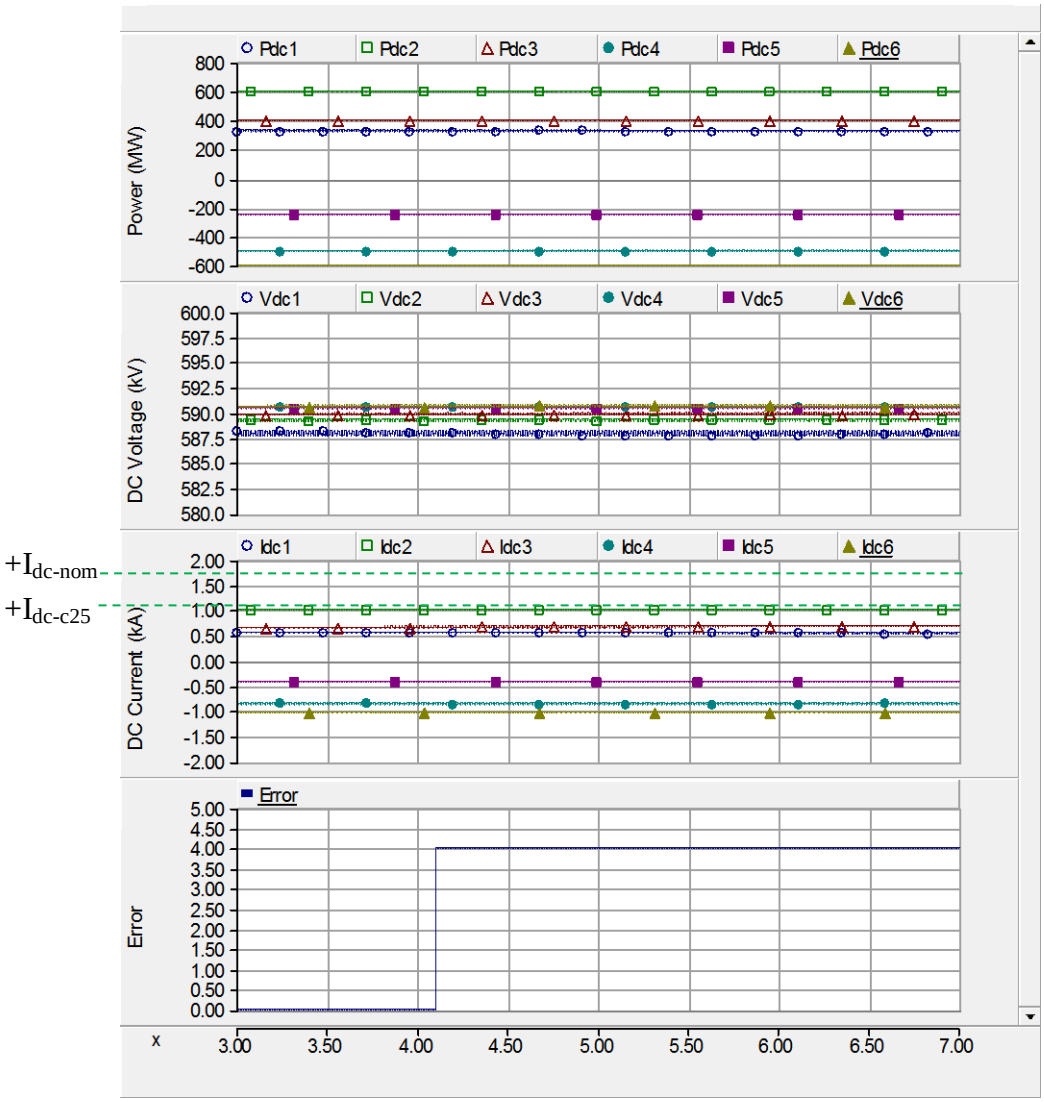

Figure 37: System's response to a cable overcurrent; x-axis is time in seconds.

6.8 Block of an onshore converter

The active power injected into the DC system by windfarms 1, 2 and 3 are approximately 500MW, 900MW and 600MW respectively. The target DC power orders for VSC2 and VSC3 are set to 1000MW and 500MW respectively and the PFS is enabled. At 5s VSC2 is blocked and the systems response is shown in Figure 38. This figure shows that VSC1 and VSC3 respond to the event by rapidly exporting more active power in order to regulate the DC voltage. It should be noted that if VSC1 and VSC3 were unable to export the active power lost by VSC2 then the DC voltage would increase until approximately 640kV, at which point the dynamic braking resistors would be enabled.

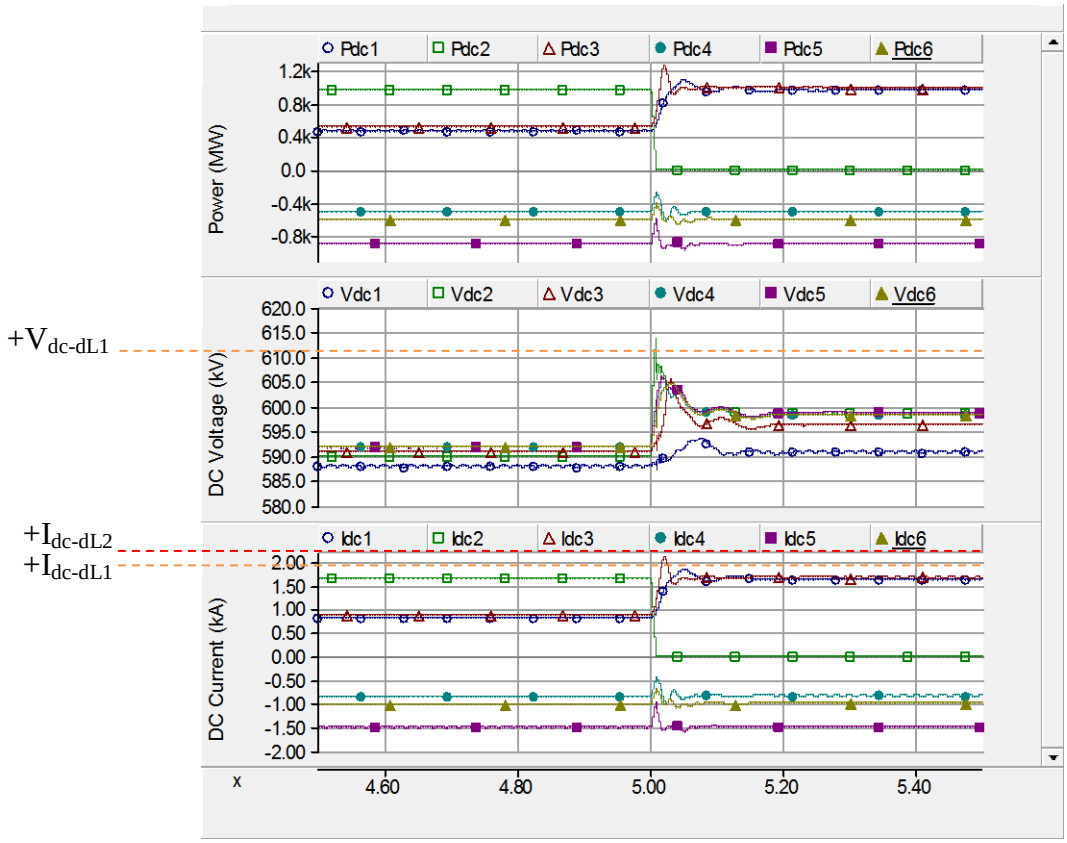

Figure 38: System's response to VSC2 being blocked at 5s; x-axis is time in seconds.

6.9 Block of an offshore converter

The active power injected into the DC system by windfarms 1, 2 and 3 are approximately 500MW, 1000MW and 500MW respectively. The target DC power orders for VSC2 and VSC3 are set to 1000MW and 500MW respectively and the PFS is enabled. At 5s, VSC5 is blocked and its AC circuit breakers are opened 40ms later. The system's response is shown in Figure 39. This figure shows that blocking VSC5 causes a deficit of 1000MW and that the DC power at the terminals of the onshore converters decreases. The PFS responds to this event at about 5.1s by controlling VSC1 to import 500MW so that VSC2 and VSC3 are able to maintain their pre-fault DC power levels.

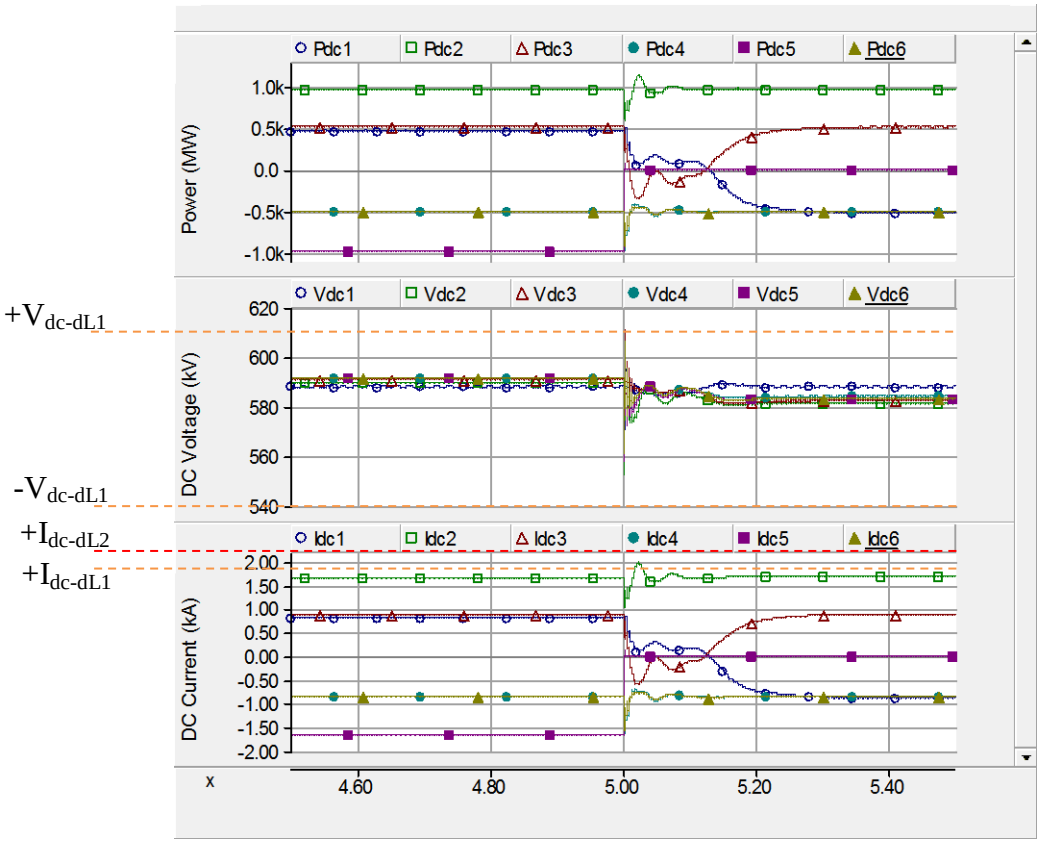

Figure 39: System's response to VSC5 being blocked at 5s; x-axis is time in seconds.

6.10 Operating Frame Test

In order to test the accuracy of the operating frame calculation method described in Section 5, the following test is conducted. VSC2 is blocked and VSC3 is set to export 980MW to the AC system. The power for all of the windfarms is initially set to 0. The target DC voltage for the PFS is set to 600kV which means that VSC1 is importing full power at the upper steady-state DC voltage limit. At 5s the active powers for windfarms 2 and 3 are increased to 400MW and 1000MW respectively and the PFS is disabled as shown in Figure 40. VSC3 exports an additional 20MW to its 1000MW limit and then VSC1 must regulate the DC voltage by exporting close to 380MW. Based on the methodology described in Section 5, the maximum DC voltage for this scenario when using a droop gain of 3.5 was calculated to be 611.33kV. The maximum simulated DC voltage was found to be 611.202kV which is close to the calculated value.

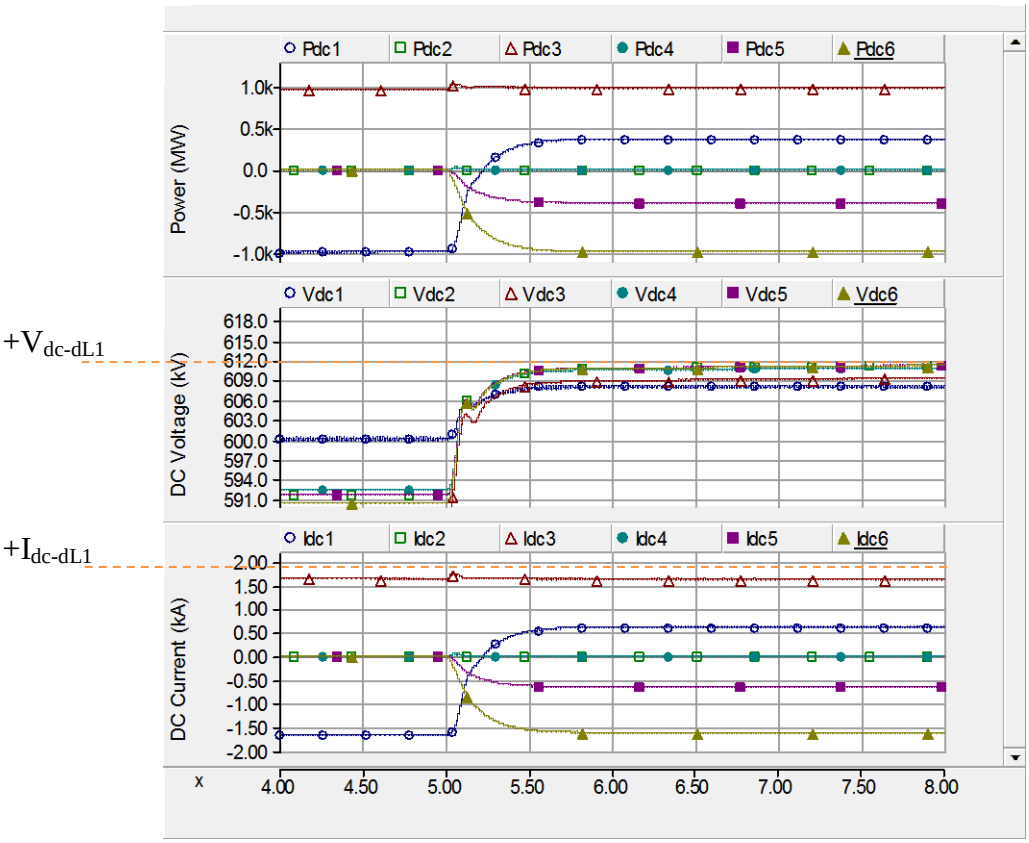

Figure 40: Operating frame test; x-axis is time in seconds.

6.11 Emergency power control

In some cases AC systems require their connected HVDC systems to provide fast active power support. In the following scenario, the AC system connected to VSC3 requests an increase of its active power level from 500MW to 1000MW at 5s. This is achieved by sending a signal to the PFS to request a new set of dispatch orders to obtain the requested power order for VSC3. The total processing and telecommunications time delays are assumed to be 12ms. Figure 41 shows that the system is able to increase the active power exported by VSC3 from 500 to 1000MW within 200ms. This response time is expected to be more than sufficient for the majority of AC systems. However, if this is considered to be too slow, the speed of the response can be improved by reducing the time constant of the first order transfer functions at the input of the ACC from their default value of 30ms. The system's response for a decrease in the active power at VSC3 from 500MW to 0MW is shown in Figure 42.

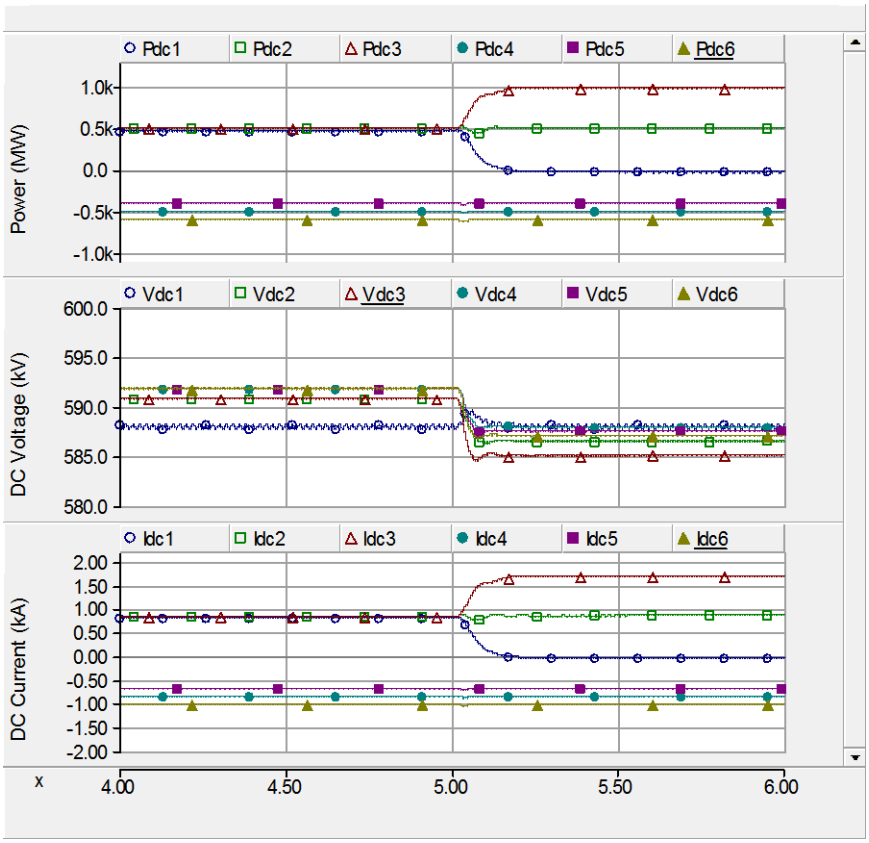

Figure 41: System's response to a power order increase for VSC3 from 500MW to 1000MW at 5s when using the PFS; x-axis is time in seconds.

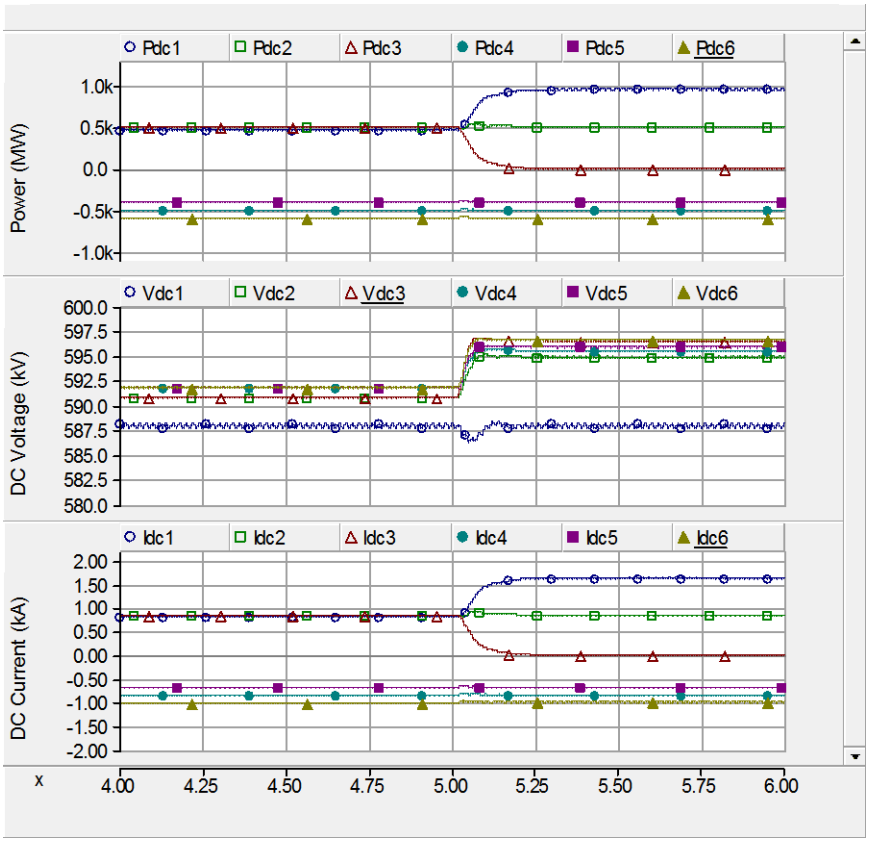

Figure 42: System's response to a power order increase for VSC3 from 500MW to 0MW at 5s when using the PFS; x-axis is time in seconds.

In the event that the emergency power support is required to work without telecommunications, the power order can be modified locally by manipulating the ACC's power order. The power set-point for the ACC at VSC3 is increased from 500MW to 1000MW at 5s and the system's response is shown in Figure 43. The active power increase at VSC3 is approximately 200MW rather than the requested 500MW. This is because manipulating the active power set-point to the ACC alone cannot accurately control active power in a DC grid.

The actual power level obtained can vary significantly depending upon the system configuration, initial operating conditions and droop constant. Figure 44 shows that the power increase for VSC3 is significantly less for the same scenario when its droop gain is decreased from 3.5 to 0.5. If accurate local power control is required without telecommunications, then another MTDC control method such as voltage margin control can offer better performance than standalone droop controllers. However, it should be noted that changing the power level locally can result in operating frame violations in other parts of the system.

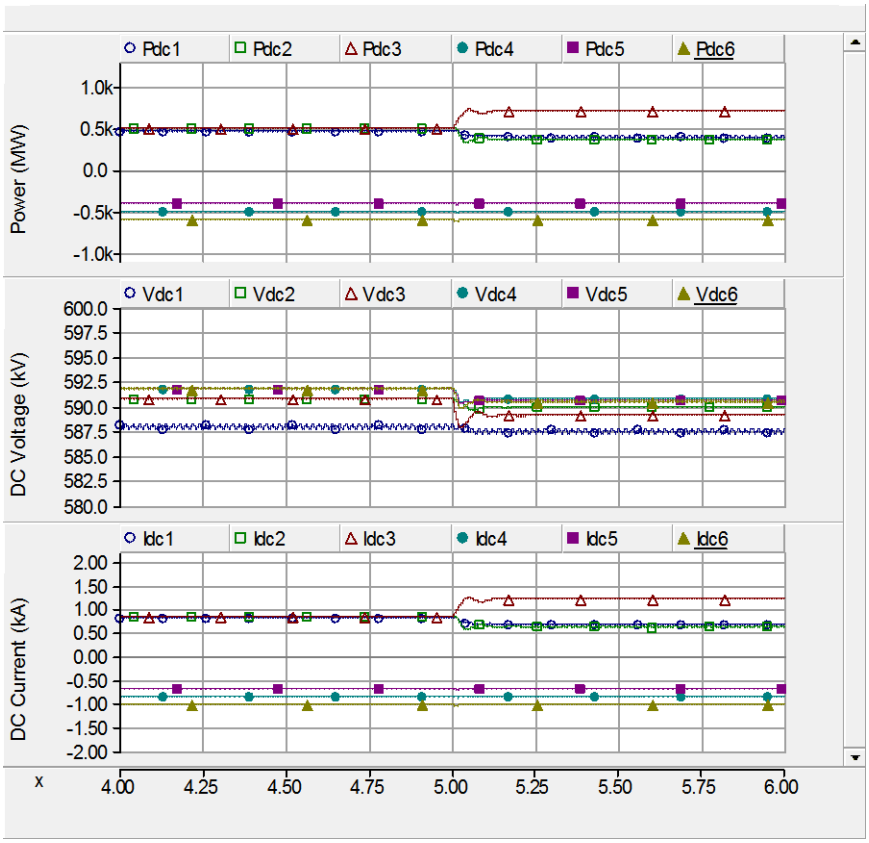

Figure 43: System's response to a power order increase for VSC3 from 500MW to 1000MW at 5s without using telecommunications; x-axis is time in seconds.

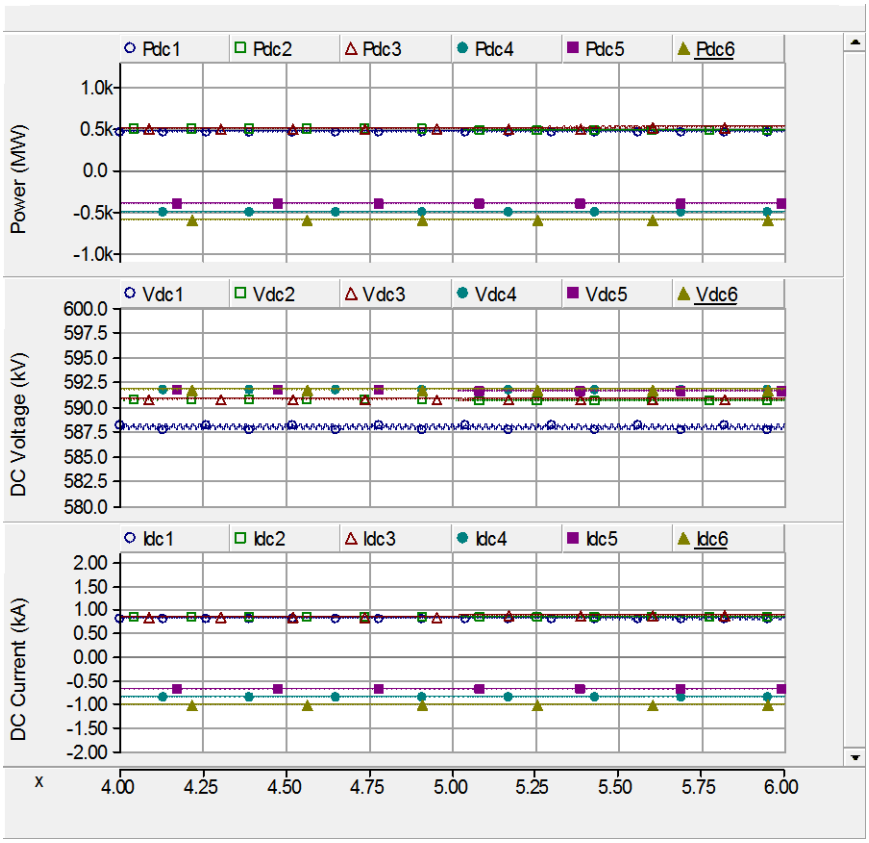

Figure 44: System's response to a power order increase for VSC3 from 500MW to 1000MW at 5s without using telecommunications and employing a droop constant of 0.5; x-axis is time in seconds.

7 Summary

This report has described the work which has been undertaken for the "DC grid control 2" Work Package. The main layers of the overall HVDC grid control architecture have been described and the key VSC control signals and their bandwidths have been defined. A power flow solver algorithm has been developed in MATLAB to calculate the node voltages required to obtain the desired DC power at each converter without exceeding the nominal operating framework for the system. Guidelines and a MATLAB algorithm have also been developed to estimate the droop gains which should be employed for the ACCs to maximise the ACCs influence on active power sharing without exceeding level 1 of the dynamic operating frame.

A model based on the DC configuration of the northern section of the Atlantic wind connection has been developed in PSCAD with all the necessary controls. A range of tests have been conducted to assess the system's steady-state and transient performance. The simulation results show that the control system is able to accurately control DC power flow in steady-state and to maintain grid stability for fast transient events without exceeding the dynamic operating limits.

8 Further work

All objectives of this work package have been met and in some areas further work has been undertaken, however significantly more work should be conducted. This section provides some recommendations for future work.

The simulation results have shown that there are some small oscillations in some of the DC traces for certain tests, the exact cause of these oscillations is unknown at this time and further investigation is therefore warranted.

The functionality and flexibility of the PFS can be improved significantly with further coding. The PFS can be made more generic in terms of the number of nodes and cables/lines which are connected to each node. It should also be modified so that any of the converters could be selected as the slack bus, by modifying the PFS matrix. Currently the PFS may not function correctly if any of the cables are disconnected. This is because setting the admittance value between nodes in the matrix to zero can result in a non-in veritable matrix. This could be solved by reconfiguring the matrix based on the network configuration. The error codes generated by the PFS should also be more extensive to give more detailed information regarding the operating frame violations. More complex algorithms could also be employed for the PFS to optimise power losses or to automatically adjust some parameters such as target DC voltage if an error code is generated.

The methodology for selecting the droop gains can also be improved by carrying out more work to determine the worst case scenarios for potential operating frame violations. This may be achieved by extending the code written for this work so that it is capable of determining the worst case scenarios.

Detailed models of the AC systems (onshore and offshore) would also enable the necessary AC/DC interactions studies to be conducted.

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Appendix A – Table of Key System Parameters

MMC-AVM	Active power rating	P	1000MW
	Reactive power rating	Q	±330MVAr
	DC voltage	V_{dc}	600kV
	DC Capacitance	C_{DC}	230μF
	Arm resistance[1]	R_{arm}	0.9Ω
	Arm inductance	L_{arm}	0.045H
Onshore MMC transformer	Leakage reactance	X_T	0.15p.u.
	Star Primary winding voltage, L-L	V_{Tp}	370kV
	Delta Secondary winding voltage, L-L	V_{Ts}	410kV
	Apparent power base	S_{base}	1000MVA
Onshore AC system	Network voltage, L-L	V_n	400kV
	Network resistance	R_n	2.28Ω
	Network inductance	L_n	0.145H
ACC	Nominal droop gain	K_{droop}	10
MMC power controllers	Proportional gain	K_p	0.000208
	Integral time constant	T_i	2.387s
MMC DC voltage controller	Proportional gain	K_p	0.0270
	Integral time constant	T_i	0.826s
MMC current controller	Proportional gain	K_p	175
	Integral time constant	T_i	0.000442s
Windfarm transformer	Leakage reactance	X_T	0.15p.u.
	Star Primary winding voltage, L-L	V_{Tp}	33kV
	Star Secondary winding voltage, L-L	V_{Ts}	220kV
Windfarm power controller	Proportional gain	K_p	0.00246
	Integral time constant	T_i	0.645s
	Windfarm time constant	τ_w	0.15s
Windfarm current controller	Proportional gain	K_p	0.327
	Integral time constant	T_i	0.29s
Offshore MMC voltage controller	Proportional gain	K_p	0.5
	Integral time constant	T_i	0.005s
	Frequency	freq	50Hz
Offshore MMC transformer	Leakage reactance	X_T	0.15p.u.
	Star Primary winding voltage, L-L	V_{Tp}	370kV
	Delta Secondary winding voltage, L-L	V_{Ts}	220kV

1. Value includes the on-state resistance of the semi-conductor devices in each arm.

Appendix B – Comparison of power flow solver equations

In this appendix, the accuracy of the power flow solver which does account for the cables' shunt conductance is compared with the standard power flow solver which does not. The cable configuration is shown in Figure 45. The VSCs are represented as DC voltage sources for this power flow study. The cables are modelled using the frequency dependent cable model with a shunt conductance value of $1x10^{-10}$S/m. Table 9.1 shows that the PFS with shunt conductance correction is more accurate than the standard PFS.

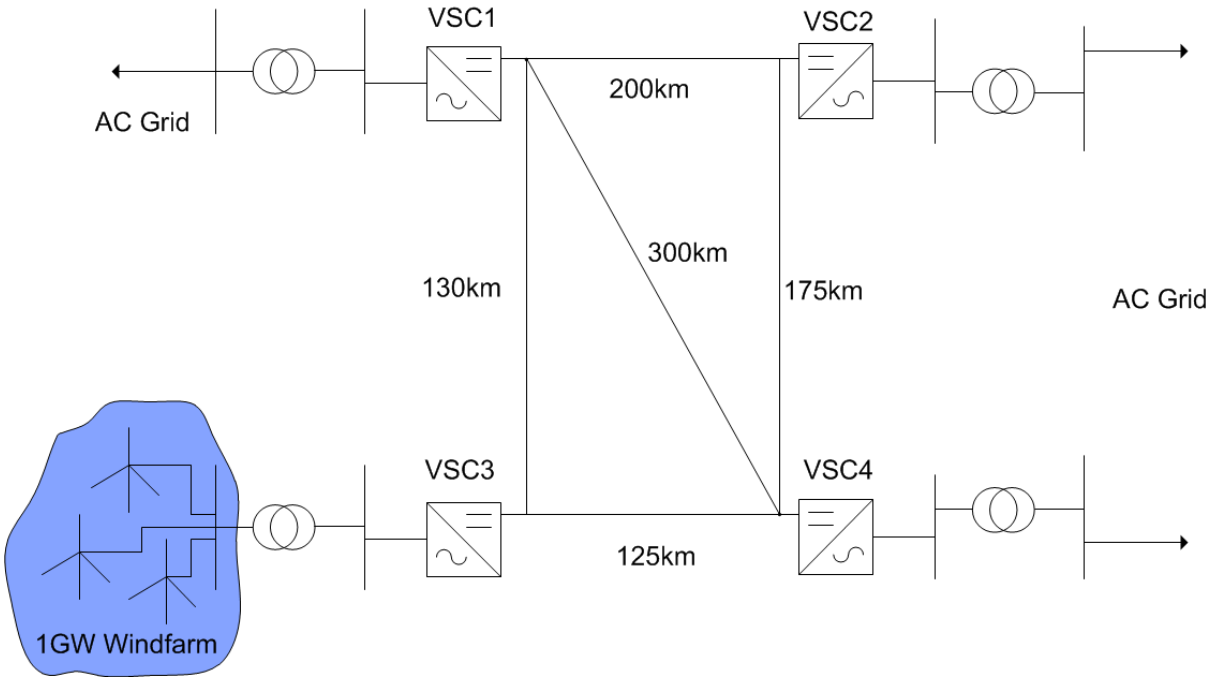

Figure 45: Four terminal PFS test model

Power Flow Solver with Windfarm power at 400MW					
VSC	-	**1**	**2**	**3**	**4**
Power Order (MW)	-	Slack	500.00	-400.00	300.00
Standard PFS	Calculated Power (MW)	-402.96	500.00	-400.00	300.00
	Calculated Voltages (kV)	600.00	597.50	600.25	598.62
	Simulated Power (MW)	-408.65	496.69	-402.34	294.65
	Error (%)	-1.41	0.66	-0.58	1.78
PFS with Shunt correction	Calculated Power (MW)	-419.70	500.00	-400.00	300.00
	Calculated Voltages (kV)	600.00	597.47	600.23	598.58
	Simulated Power (MW)	-419.72	500.04	-400.01	300.00
	Error (%)	-0.01	-0.01	0.00	0.00

Table 9.1: Comparison between the standard PFS and the PFS with shunt conductance correction.

Appendix C– Derivation of operating point equations

The set-point for the DC voltage controller is calculated according to equation (57).

$$V_{dco} = \left(I_{dc} - I_{dc}*\right) K_{droop} + V_{dc}* \tag{57}$$

Where:

$$I_{dc}* = P_{dc}* / LRSP \tag{58}$$

$$V_{dc}* = LRSP \tag{59}$$

Multiplying both sides by I_{dc} gives equation (60).

$$P_{dc} = I_{dc}{}^{2} K_{droop} - I_{dc}(I_{dc}* K_{droop} - V_{dc}*) \tag{60}$$

Noting that $I_{dc}* = I_{dc-op1}, V_{dc}* = V_{dc-op1}, P_{dc} = P_{dc-op2}$ and $I_{dc} = I_{dc-op2}$, the solution to $I_{dc\text{-}op2}$ is given by equation (61).

$$I_{dc-op2} = \frac{\sqrt{(4 \times K_{droop} \times P_{op2} + A^2)} + A}{2 \times K_{droop}} \tag{61}$$

Where:

$$A = I_{dc-op1} \times K_{droop} - V_{dc-op1} \tag{62}$$

Hence the DC voltage at the new operating point (OP2) is given by equation (63).

$$V_{dc-op2} = \left(I_{dc-op2} - I_{dc-op1}\right) \times K_{droop} + V_{dc-op1} \tag{63}$$

Appendix D – Control architecture with operating frame

This diagram shows the overall control architecture and the different control layers which have the greatest influence on the different operating frame limits.